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# MS-B9091 Ver: 1.0

## Intel - Kabylake Platform

### CPU:

Intel Kabylake-K Series Processor **Max 95 Watt.**

### System Chipset:

Intel Kabylake PCH-Z270

### OnBoard Chipset:

e-SIO : NUVOTON/NCT6685D

HD Audio Codec : REALTEK/ALC1150

AUDIO AMPLIFY : TI TPA6132A

LAN : Killer LAN E2500

### Main Memory:

DDR4 SO\_DIMM 1600MHZ \* 2

### Expansion Slots:

PCIE x 16 \*1

M.2 E-key PCIE 1X \* 1

M.2 M-Key PCIE 4X \* 1 (only PCIE\*4)

M.2 M-Key PCIE 4X \* 2 (Auto switch SATA\*1/PCIE\*4)

### PWM:

Controller : ON Semiconductor/NCP81203MNTXG 6 + 2 Phase

### Other:

SATA\*4

Rear USB 2.0 \*2

Rear USB 3.0 \*4

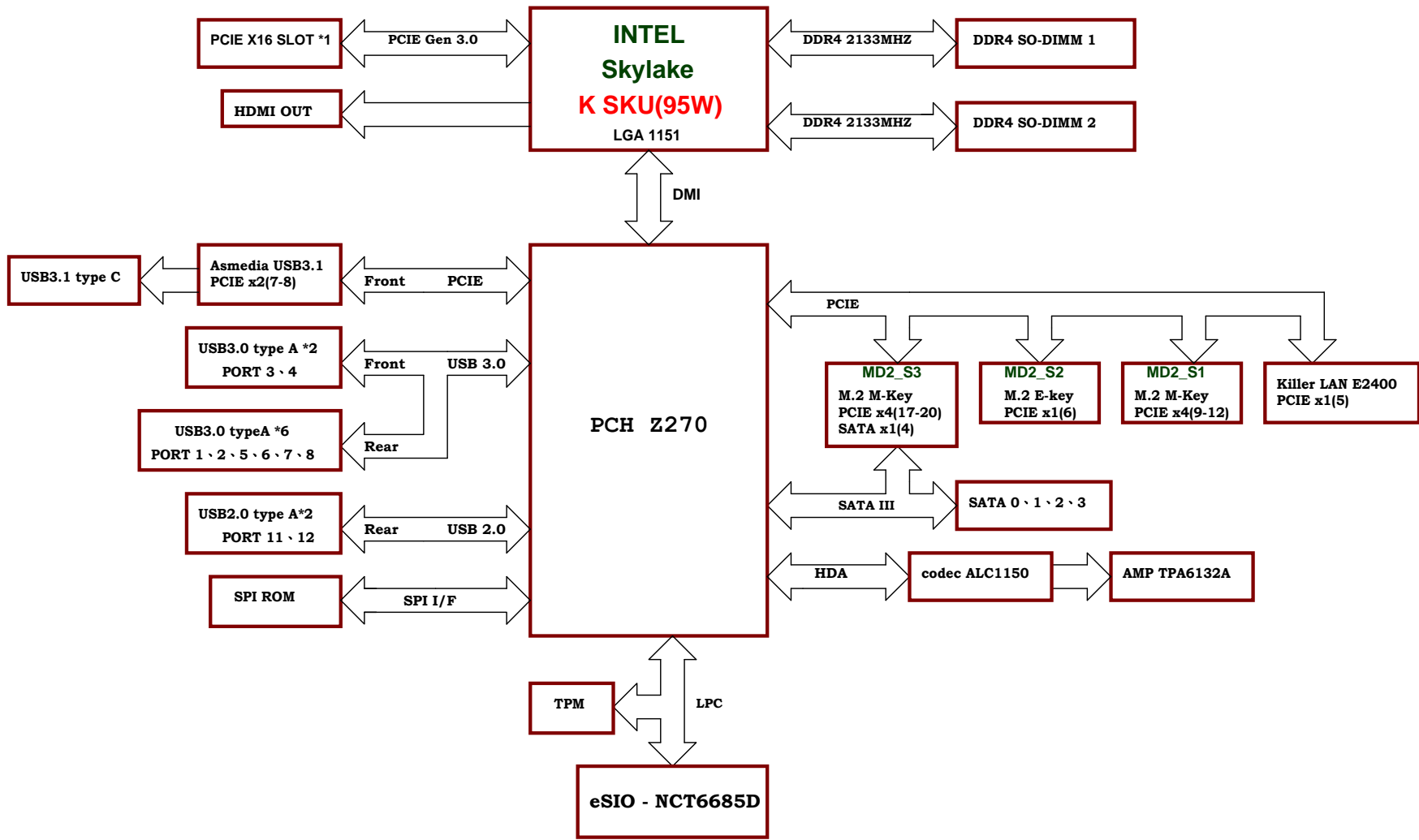
HDMI OUT\*1

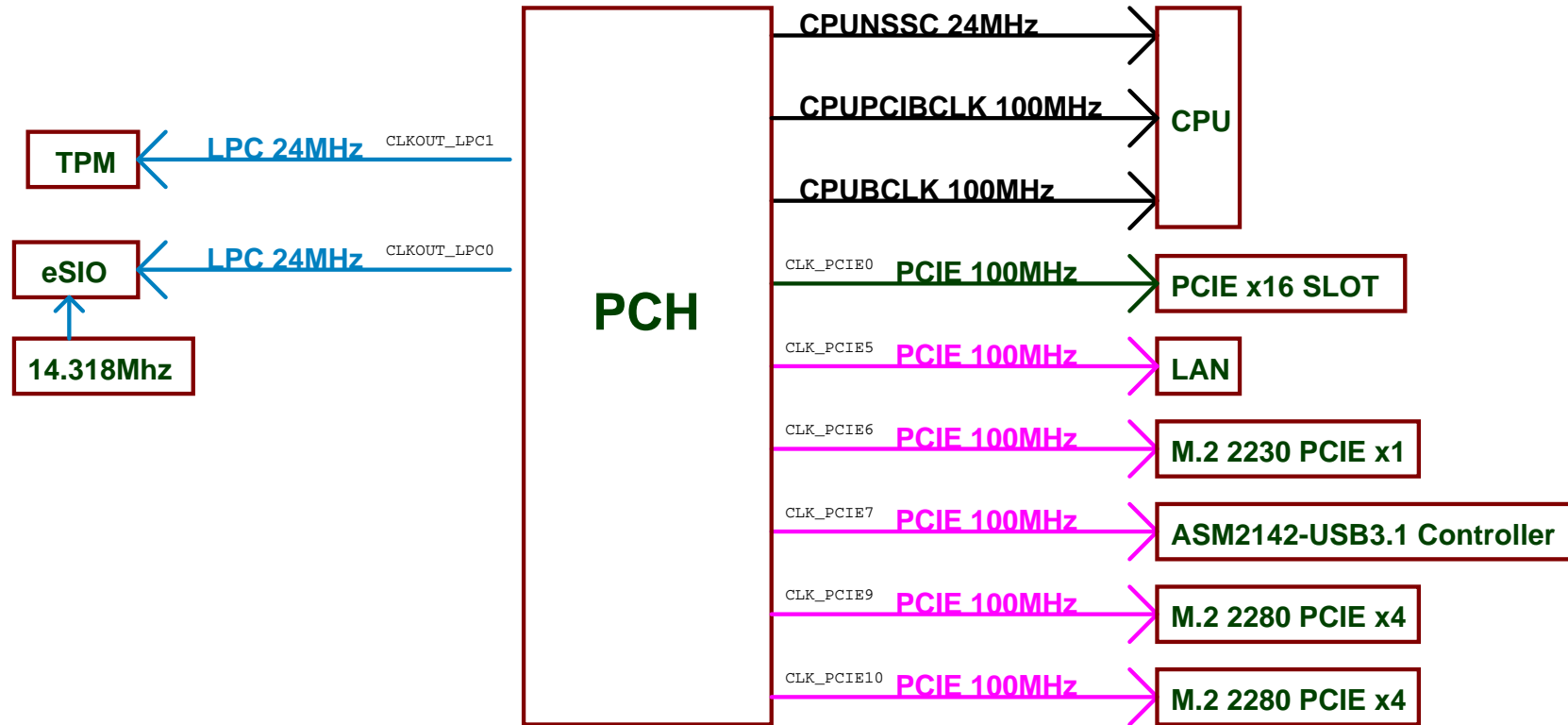
Front USB 3.0 typeA \*2(1port support QC2.0)

Front USB 3.0 typeC \*1



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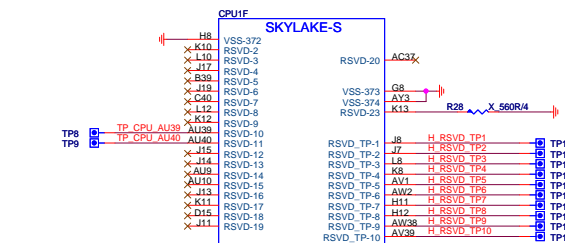
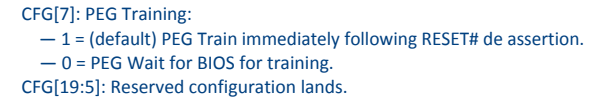




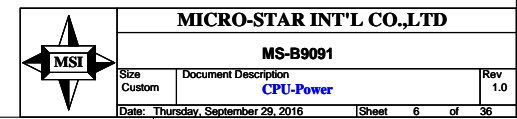
**MICRO-STAR INT'L CO.,LTD**

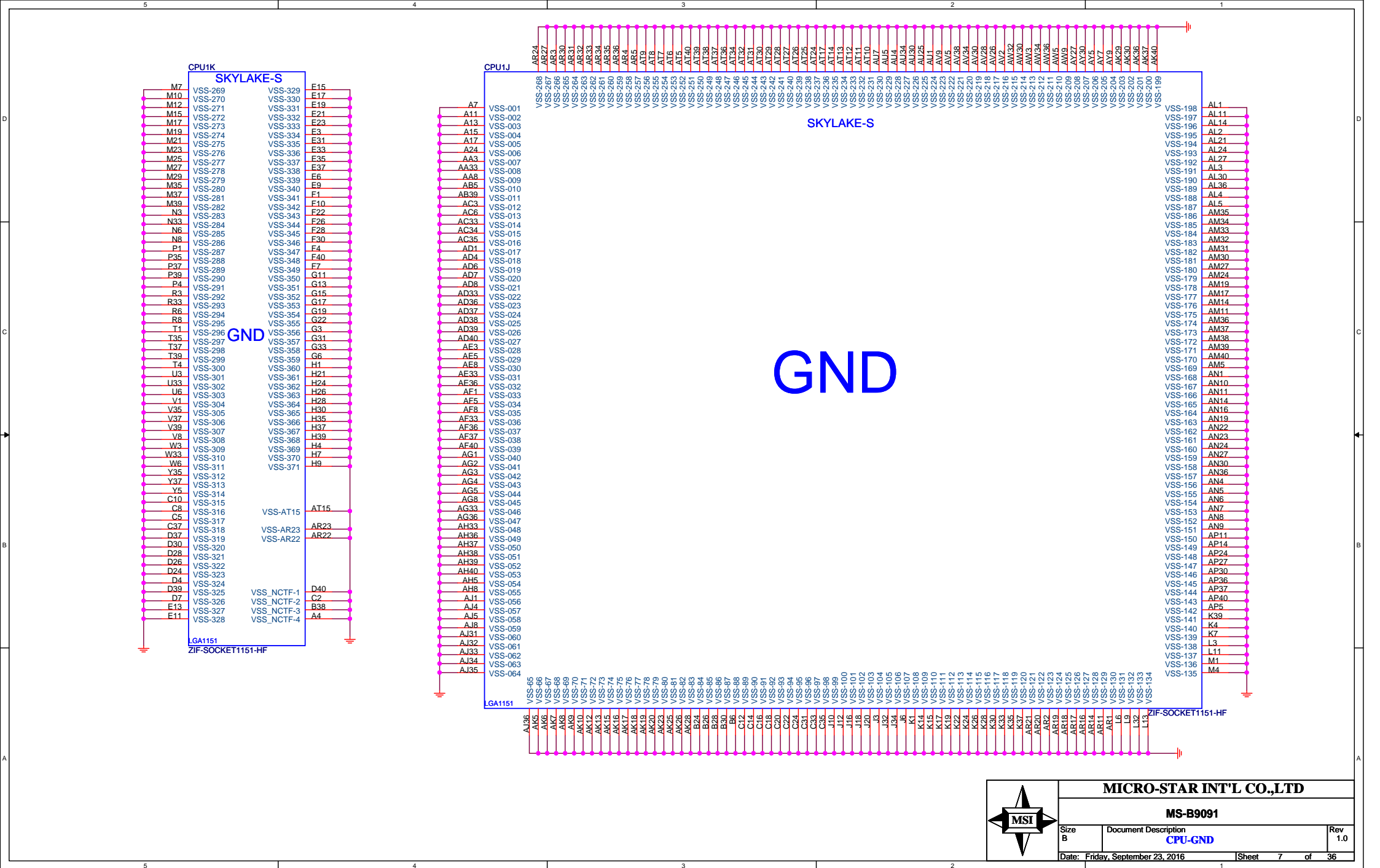
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Size B	Document Description <b>Clock Distribution</b>	Rev 1.0
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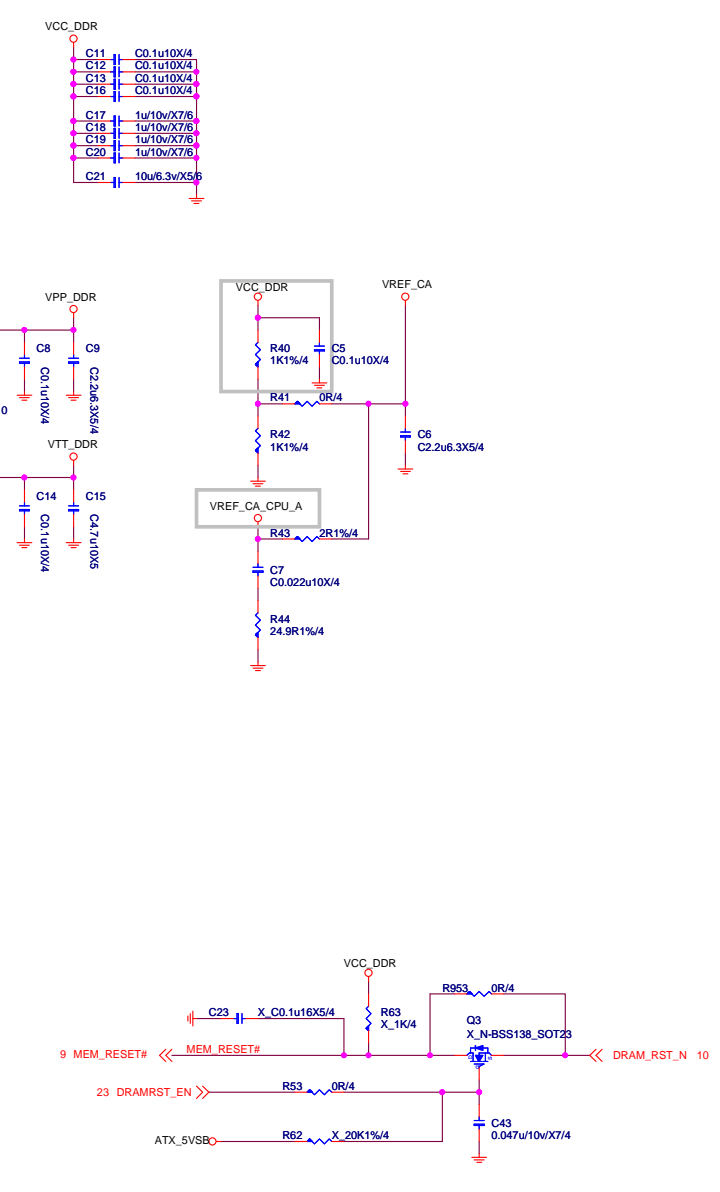
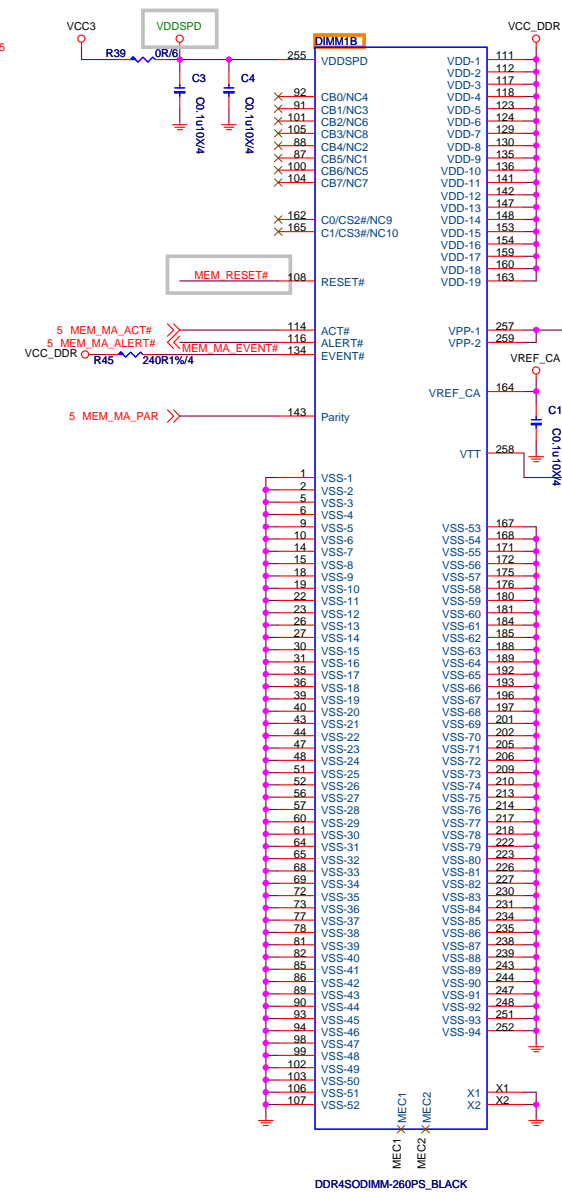
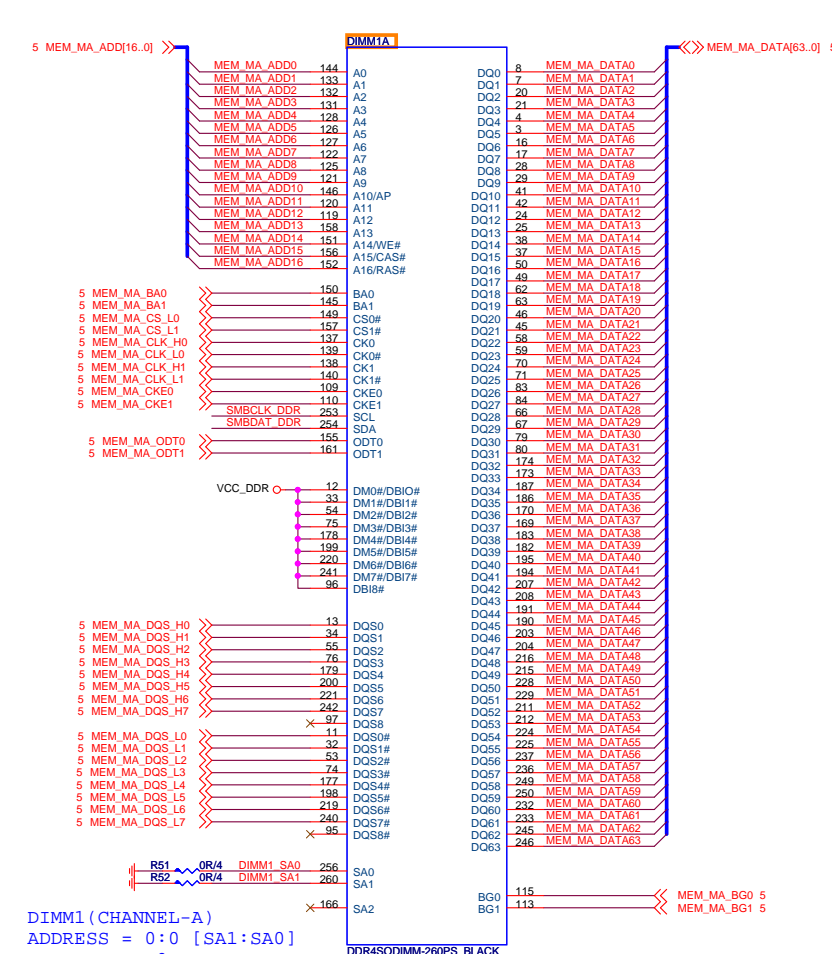




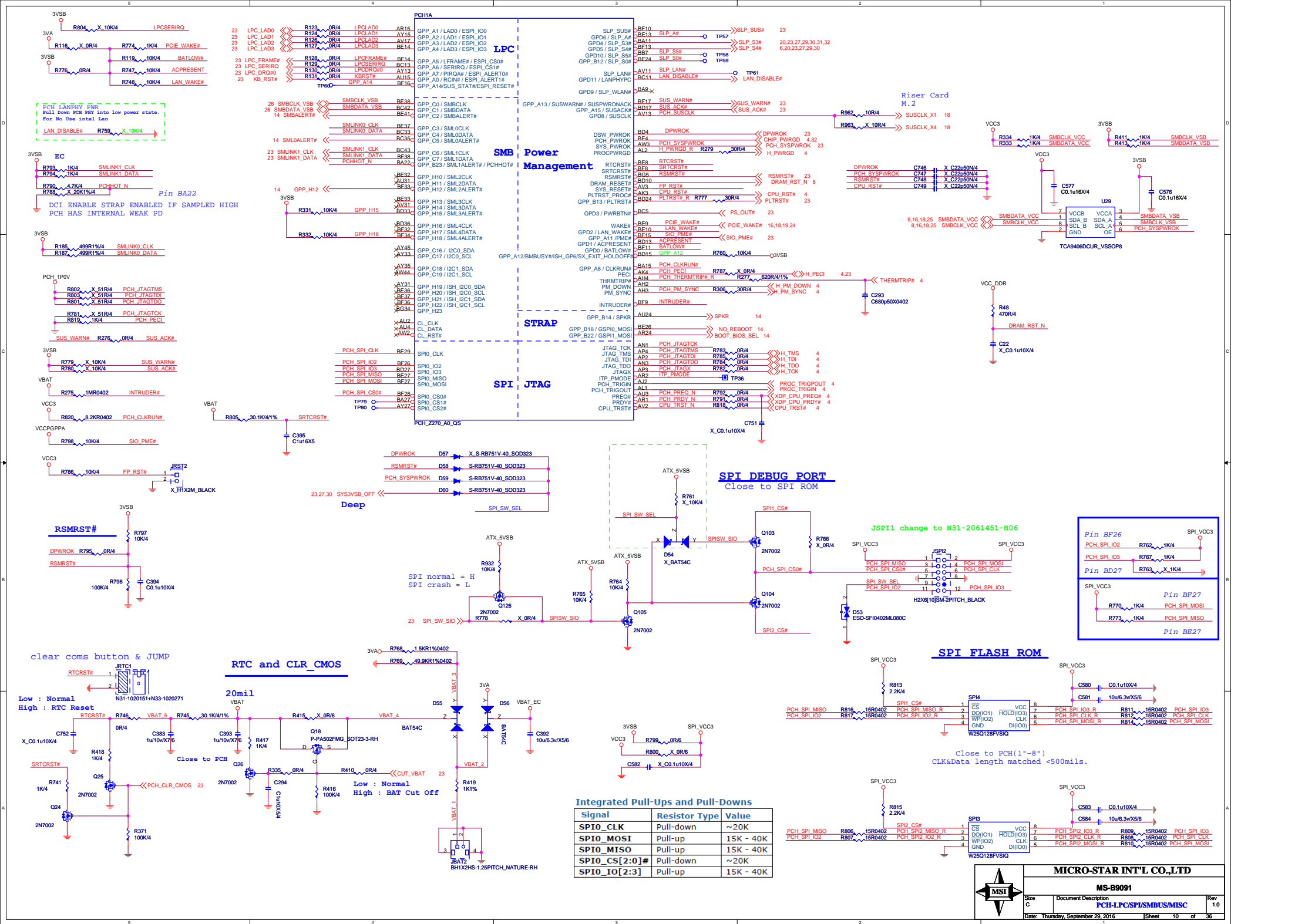


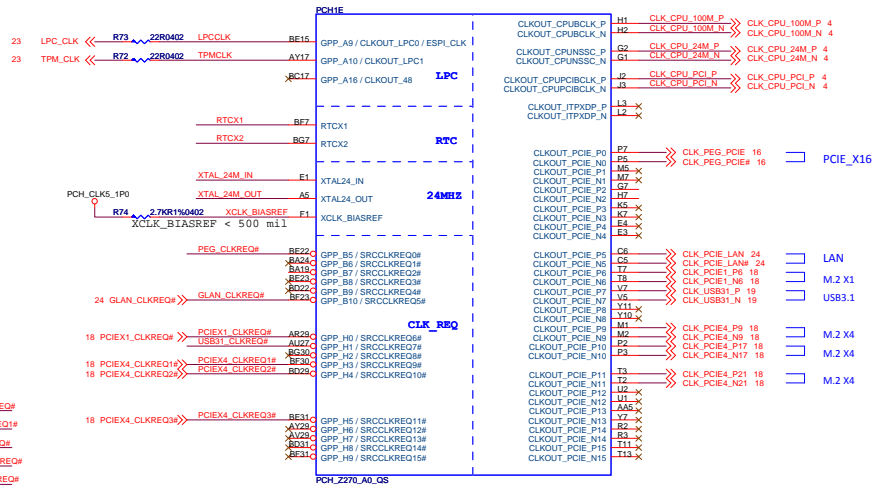


DDR4 SO-DIMM DIMM1







[illegible]

Parameter	Symbol	Recommended Value	Max/Min Range	Condition
Frequency	$f_0$	24MHz		@25°C
Vibration Mode		Fundamental		
CUT		AT		
Loading		Parallel resonant		
Frequency Tolerance @25C	$Df/f_0$ @25°C	±35ppm		@25°C ±3°C

Parameter	Symbol	Recommended Value	Max/Min Range	Condition
Temperature Stability	$Df/f_0$	±30ppm		10° to 70°C
Aging	$Df/f_0$	±5ppm		
Crystal Loading	$C_{load}$	18-20pF		
Shunt capacitance	$C_0$		6pF Max	
Drive Level	$D_L$		200uW Min	
Series Resistance	$R_S$		50Ω or less	@25°C

**Note:**

- Customers should verify that the vendor's published specifications in the component data sheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective data sheet.
- Perform conformance testing and EMC (FCC and EN) testing in real systems
- Independently measure the component's electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.

Pin Name	Recommendation
DDPB_AUXP DDPC_AUXDDPD_AUXPP	No Connect
DDPB_AUXN DDPC_AUXN DDPD_AUXN	No Connect
DDPB_HPD DDPC_HPD DDPD_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0] DDI3_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0] DDI3_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK DDPC_CTRLDATA	No Connect
DDPD_CTRLCLK DDPD_CTRLDATA	No Connect

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect

The diagram illustrates the PCH - H interface. On the left, a 1.0V supply is connected to a 2.71 K $\Omega$  resistor, which is connected to the XCLK\_BIASREF pin. The PCH - H block has several output pins (indicated by dashed arrows) connecting to various components:

- CLKOUT\_C\_PUNSCC\_PIN to Processor
- CLKOUT\_C\_PUBCLK\_PIN to Processor
- CLKOUT\_C\_PUBPBCCLK\_PIN to Processor
- CLKOUT\_ITPXPDP\_PIN to ITP/XDP Port
- CLKOUT\_LPC1[0] to LPC/24MHz Device Endpoint
- CLKOUT\_48 (NBL\_PCH-H Server Only) to 48MHz Device Endpoint
- CLKOUT\_POE\_PIN[15:0] to 100MHz Endpoint
- SRCLKREQ[15:0] to 100MHz Endpoint
- XTAL24\_IN and XTAL24\_OUT to the OSC (Oscillator)

The OSC is a 24 MHz +/- 30 PPM oscillator.

	<p>Any used, enabled, and mapped SRCLKREQ# signal should connect to a PCIe* connector pin or a device down ball with a 10K Ohm <math>\pm 10\%</math> external pull-up resistor to core rail.</p> <p><u>Any un-used, disabled, and non-mapped SRCLKREQ# signal must be left as no connects at the PCH side on the platform.</u></p>
SRCLKREQ#[15:0]	<p>Notes:</p> <ul style="list-style-type: none"> <li>• The SRCLKREQ#[15:0] signals can be configured to map to any of the PCI Express* Root Ports</li> <li>• SRCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements             <ul style="list-style-type: none"> <li>— SRCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs</li> <li>— SRCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs</li> </ul> </li> </ul>

22pF +/-10%

C<sub>e1</sub>

C<sub>Load</sub>

24MHz

1M Ohm +/- 1% Bias Resistor

M

BO2

BO1

XTAL24\_IN

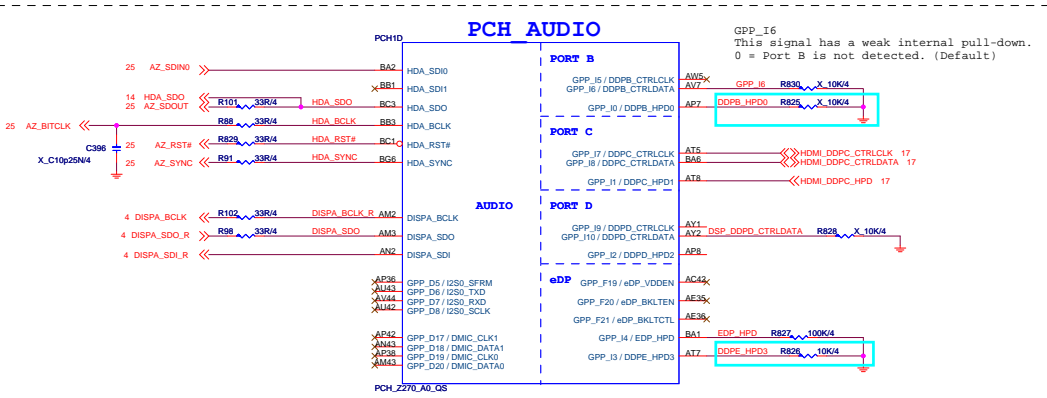
PCH - H

XTAL24\_OUT

C<sub>e2</sub>

564413\_KBL\_SKL\_U\_24\_MHz

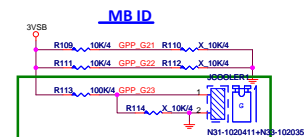
電容 GND 不能下





**MB ID**

GPP_G21	GPP_G22	GPP_G21	BOM P/N
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



Features			Q250	H270	B250	Z270	Q270
Intel® Rapid Storage Technology			AHCI Mode	Full Features <sup>1</sup>	AHCI Mode	Full Features <sup>1</sup>	Full Features <sup>1</sup>
Total USB 3.0 Ports			8	8	6	Up to 10	Up to 10
			14 <sup>3</sup>	14 <sup>3</sup>	12 <sup>2</sup>	14 <sup>3</sup>	14 <sup>3</sup>
Total SATA 6 Gb/s (Gen3) Ports			Up to 6	Up to 6	Up to 6	Up to 6	Up to 6
Total PCI Express* 3.0 Lanes			Up to 14	Up to 20	Up to 12	Up to 24	Up to 24
Total Controllers for Intel® RST for PCIe* Storage Devices			1	2 <sup>4</sup>	1	3 <sup>5</sup>	3 <sup>5</sup>
Processor PCI Express* 3.0 Lanes Configuration Support			1x16	1x16	1x16	1x16 or 2x8 or 1x8+2x4	1x16 or 2x8 or 1x8+2x4
Processor Over clocking			No	No	No	No	Yes

**Notes:**

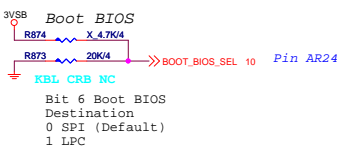
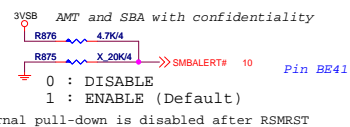
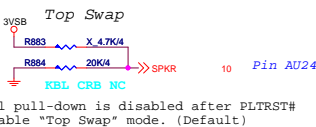
1. Full featured includes SATA RAID 0/1/5/10 support
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. Intel® RST PCIe\* supports RAID configuration 0/1/5
5. Intel® RST PCIe\* supports RAID configuration 0/1/5

				or GPI		straps are loaded	
GPP_F3	None	No	Yes (Note 4)	SATAXPICIE (1st) / SATAP6 (2nd) (Server/WS Only)	SATAXPICIE / SATAP6 or GPI	None	Default SATAXPICIE is set by a soft strap. Default is GPI before soft straps are loaded
GPP_F4	None	No	Yes (Note 4)	SATAXPICIE (1st) / SATAP7 (2nd) (Server/WS Only)	SATAXPICIE / SATAP7 or GPI	None	Default SATAXPICIE is set by a soft strap. Default is GPI before soft straps are loaded

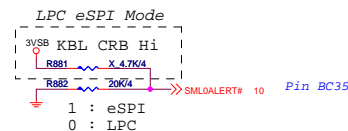
Table 9-1. Functional Strap Definitions

	Signal	Usage	When Sampled	Comment	Signal	Usage	When Sampled	Comment			
b	SPKR/GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "Top Swap" mode. (Default)</p> <p>1 = <b>Enable</b> "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. Software will not be able to clear the Top Swap bit until the system is rebooted.</li><li>3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).</li><li>4. This signal is in the primary well.</li></ol>	SPI0_MOSI	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>			
				SPI0_MISO	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				
				SMLALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-down.</p> <p>This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p><b>Note:</b> When used as PCHHOT#, a 150k weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling.</p>				
				SPI0_IO2	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>				
c	GSP10_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode. (Default)</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>	SPI0_IO3	Reserved	Rising edge of RSMRST#	<p>This signal has an internal pull-up.</p> <p>This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p>			
				SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel ME Cryptographic Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = <b>Enable</b> Intel ME Cryptographic Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel® SBA (Intel® Small Business Advantage) with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after RSMRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>	HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Enable</b> security measures defined in the Flash Descriptor. (Default)</p> <p>1 = <b>Disable</b> Flash Descriptor Security (<b>override</b>). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.</li><li>3. This signal is in the primary well.</li></ol>
							DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected. (Default)</p> <p>1 = Port B is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>	
							DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected. (Default)</p> <p>1 = Port C is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>	
→	GSP11_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).</p> <p><b>Bit 6      Boot BIOS Destination</b></p> <p>0      SPI (Default)</p> <p>1      LPC</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.</li><li>3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.</li><li>4. This signal is in the primary well.</li></ol>	DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port D is not detected. (Default)</p> <p>1 = Port D is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>			
				SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>LPC</b> is selected for EC. (Default)</p> <p>1 = <b>eSPI</b> is selected for EC.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>1. The internal pull-down is disabled after RSMRST# de-asserts.</li><li>2. This signal is in the primary well.</li></ol>	GPP_H12	Reserved	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p><b>Note:</b> The pull-down resistor is disabled after RSMRST# de-asserts</p>

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This Signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).



ESPI/LPC SELECT STRAP  
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC  
PCH HAS INTERNAL WEAK PD



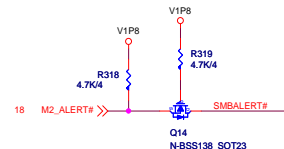
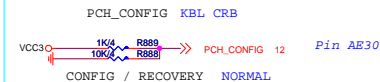
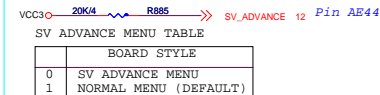
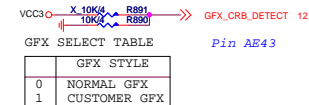
This signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor. (Default)  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.



This signal has a weak internal pull-down.  
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

## Straps

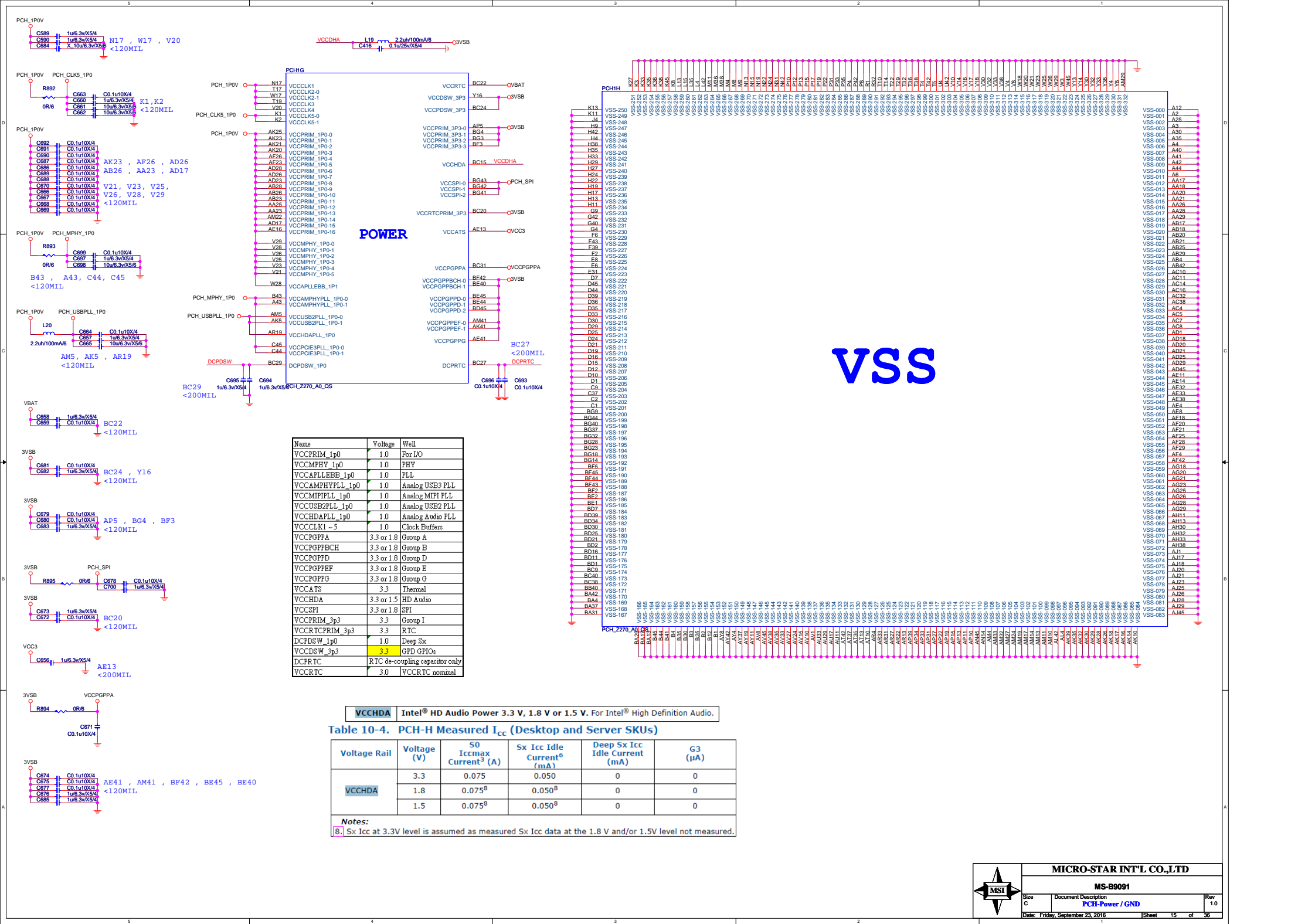
KBL CRB Page 54



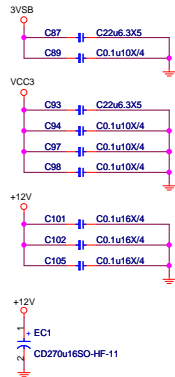
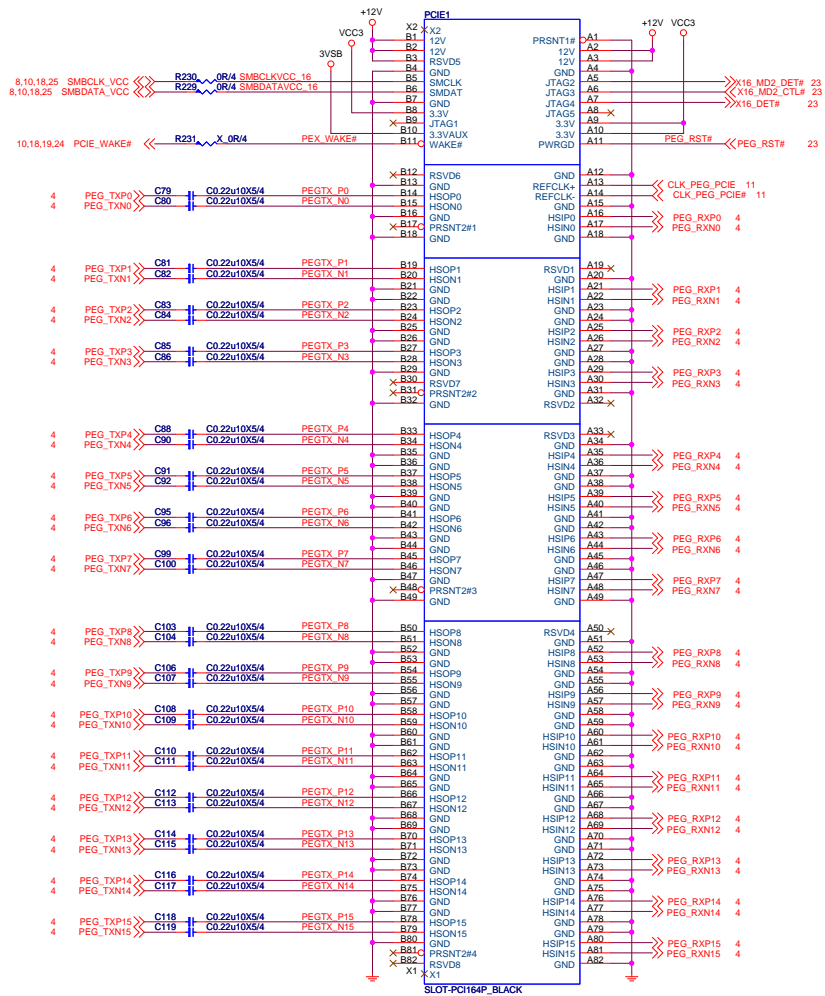
MICRO-STAR INT'L CO.,LTD

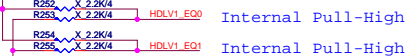
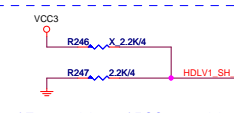
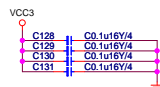
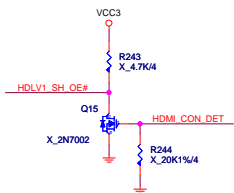
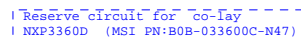
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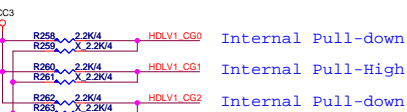


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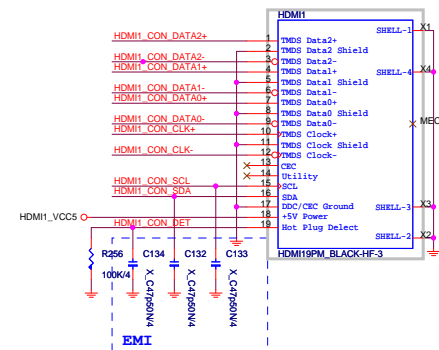
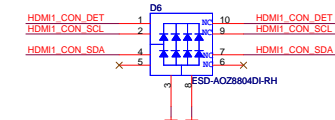
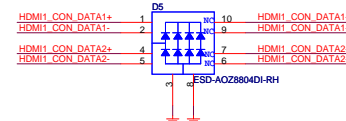
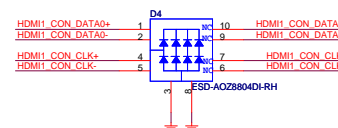
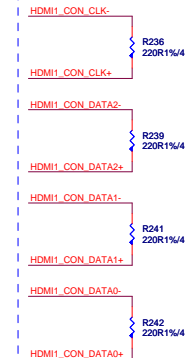
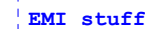
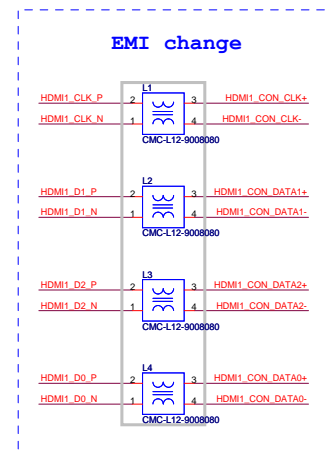
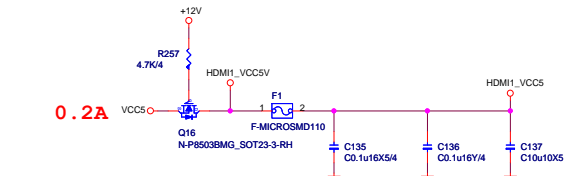
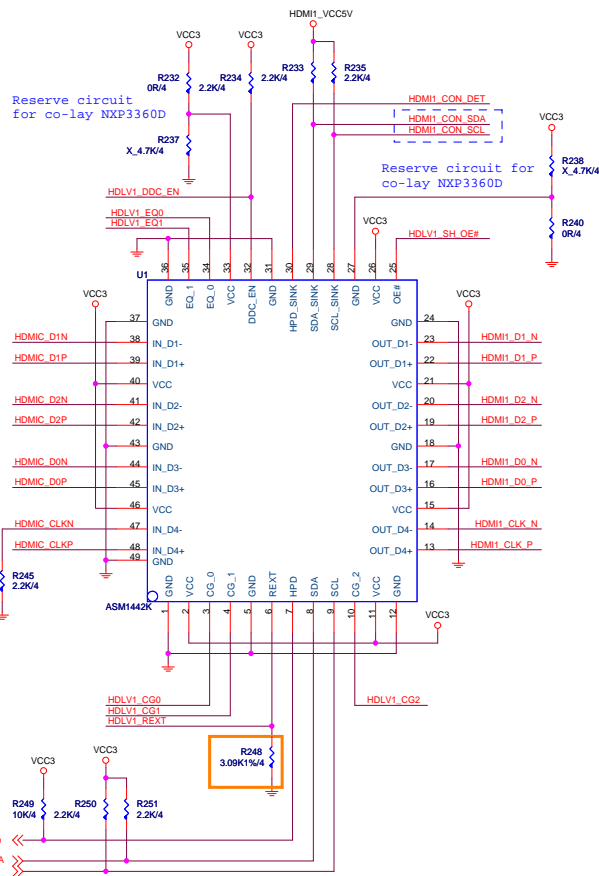


EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

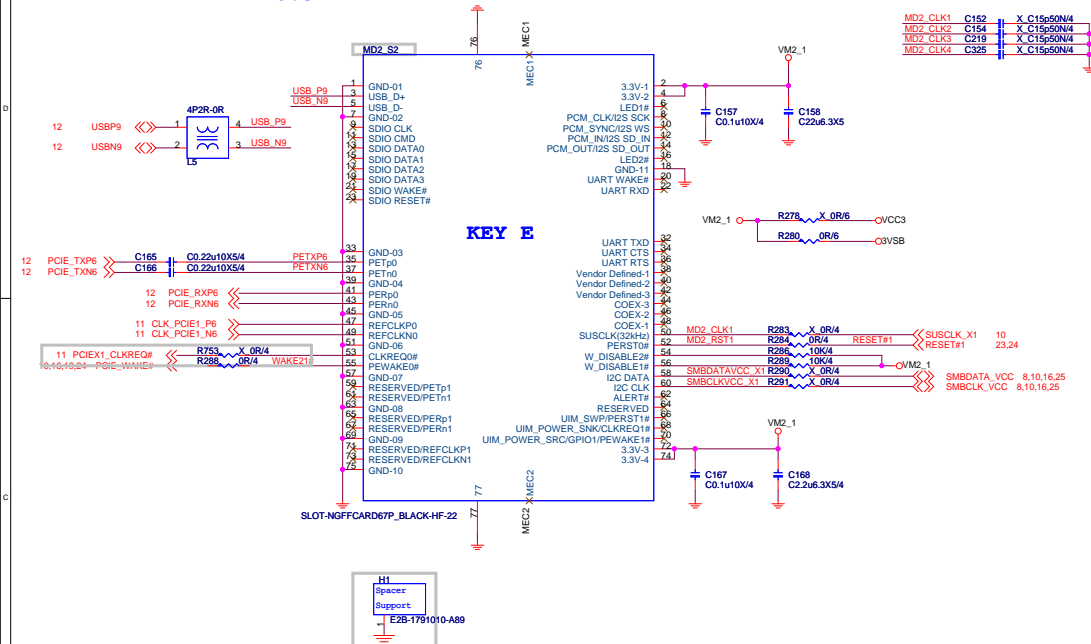


訊號強度增強 , 1 1 1

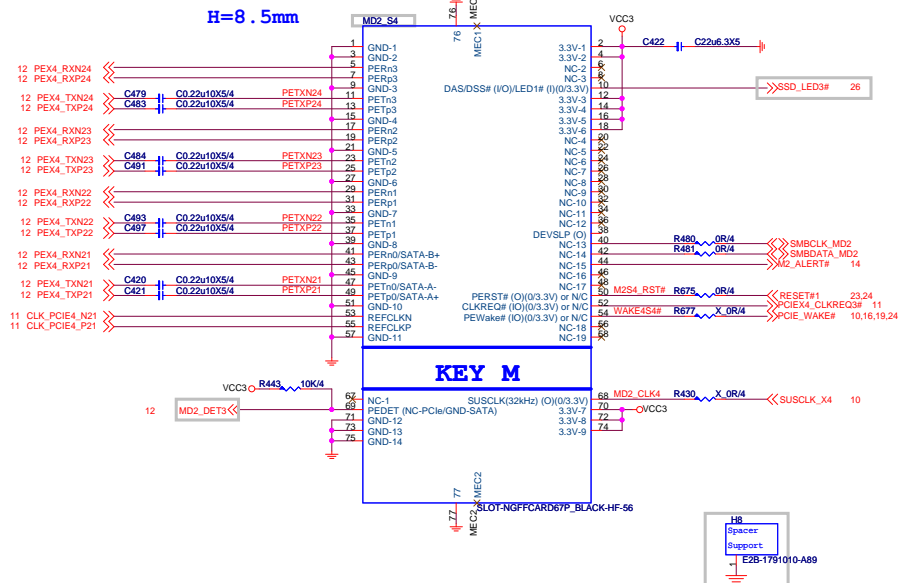
CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
1	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	



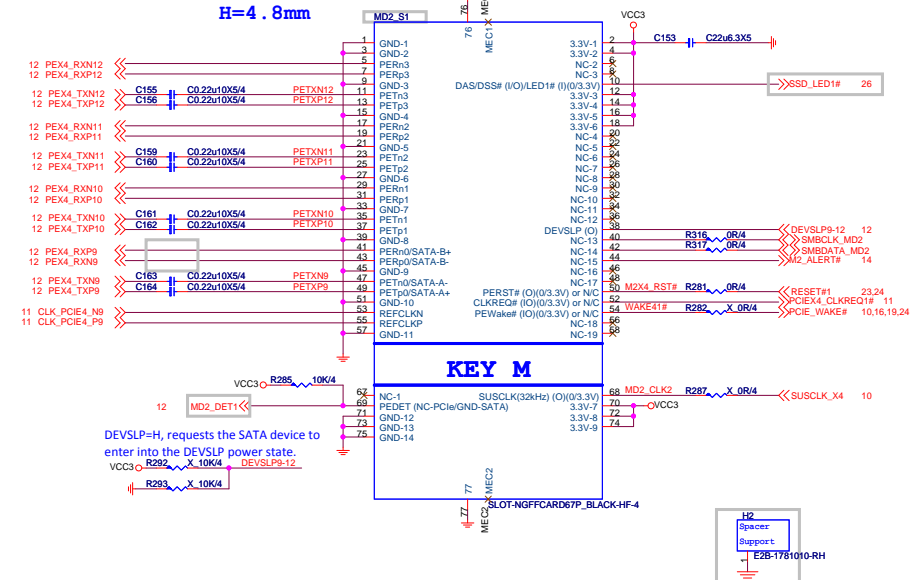
H=8 . 5mm



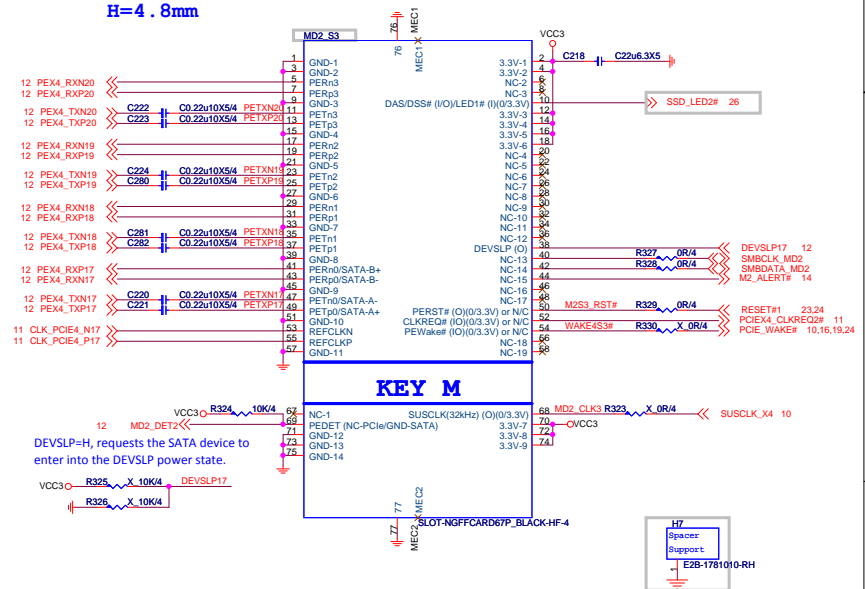
H=8.5mm



H=4 . 8mm



H=4 . 8mm

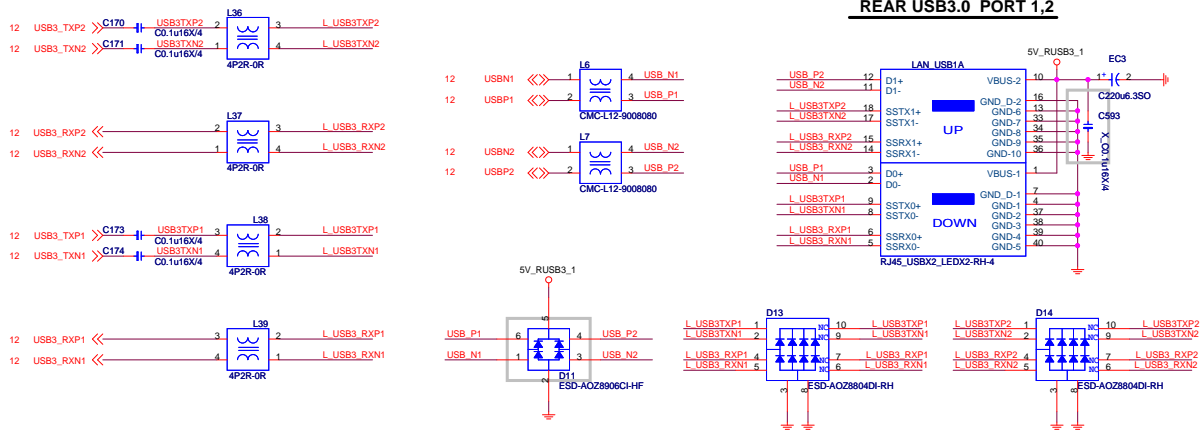


**MICRO-STAR INT'L CO.,LTD**

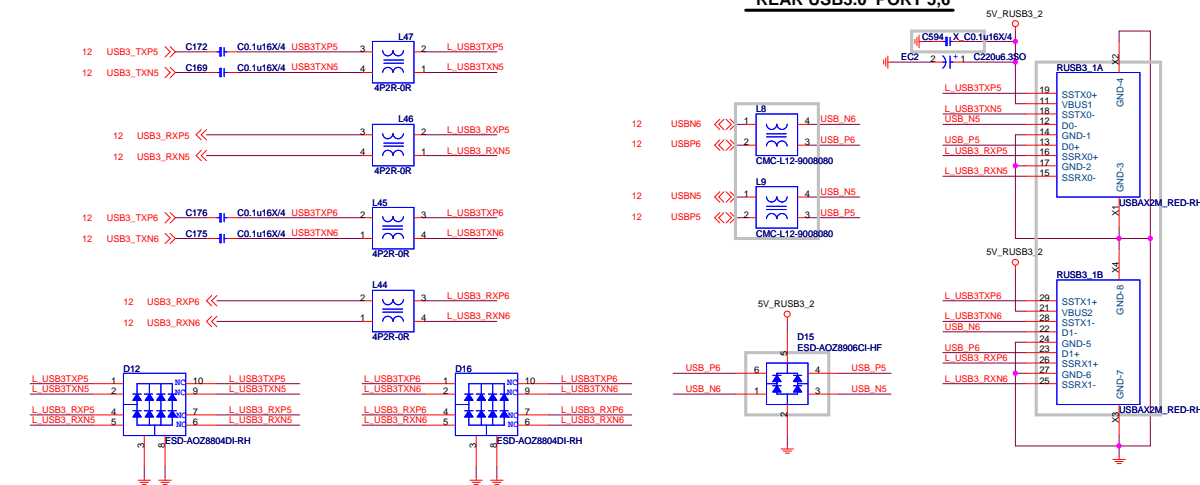
MS-B9091

Size C	Document Description <b>M.2 Slot</b>	Rev 1.0
Date: Thursday, September 29, 2016		Sheet 18 of 36

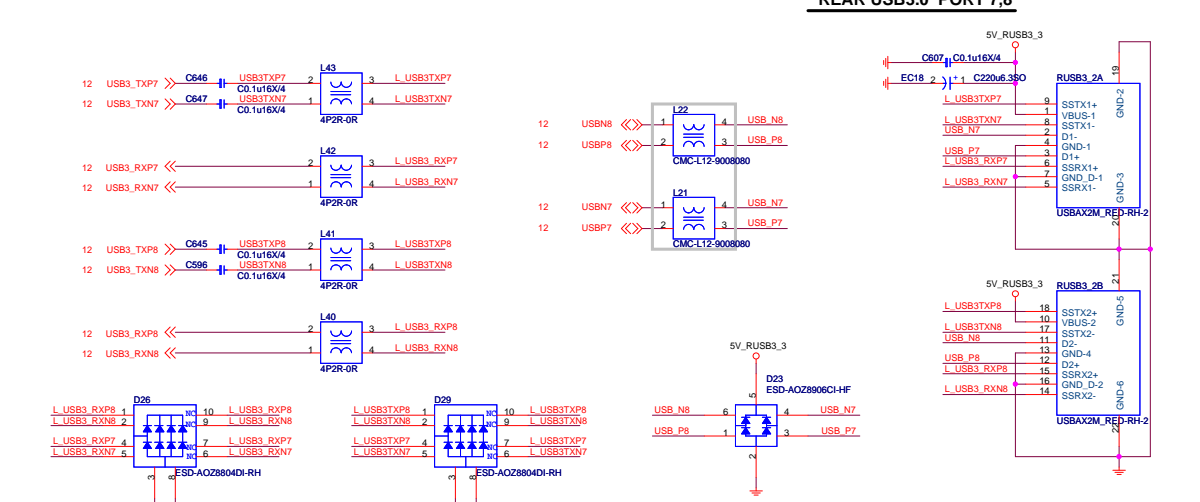
**REAR USB3.0 PORT 1,2**



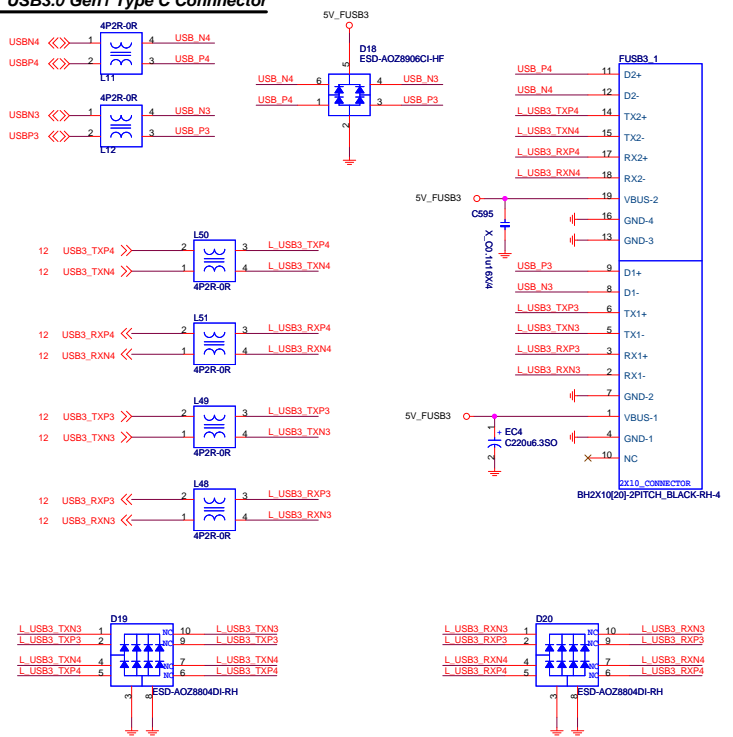
**REAR USB3.0 PORT 5,6**



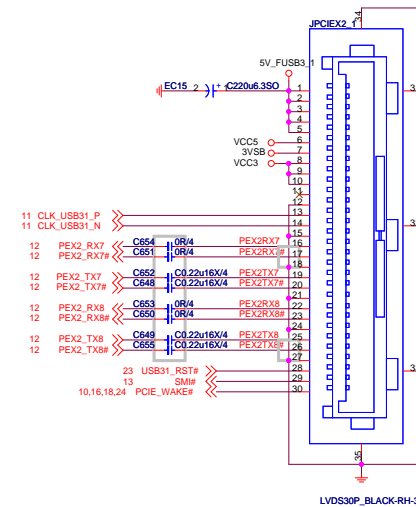
**REAR USB3.0 PORT 7,8**



### FRONT USB3.0 Gen1 Type C Connector



**FRONT PCIEx2 connector for ASM1142 USB3.1**

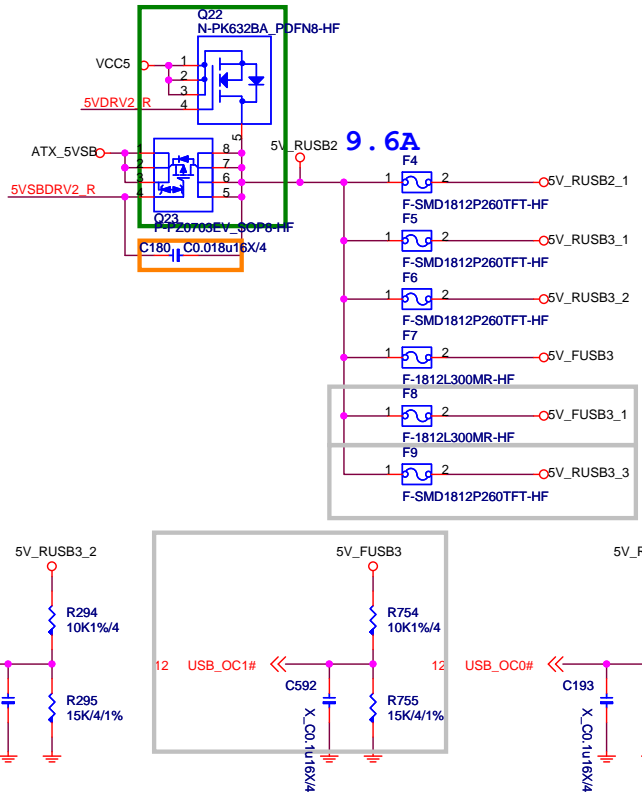
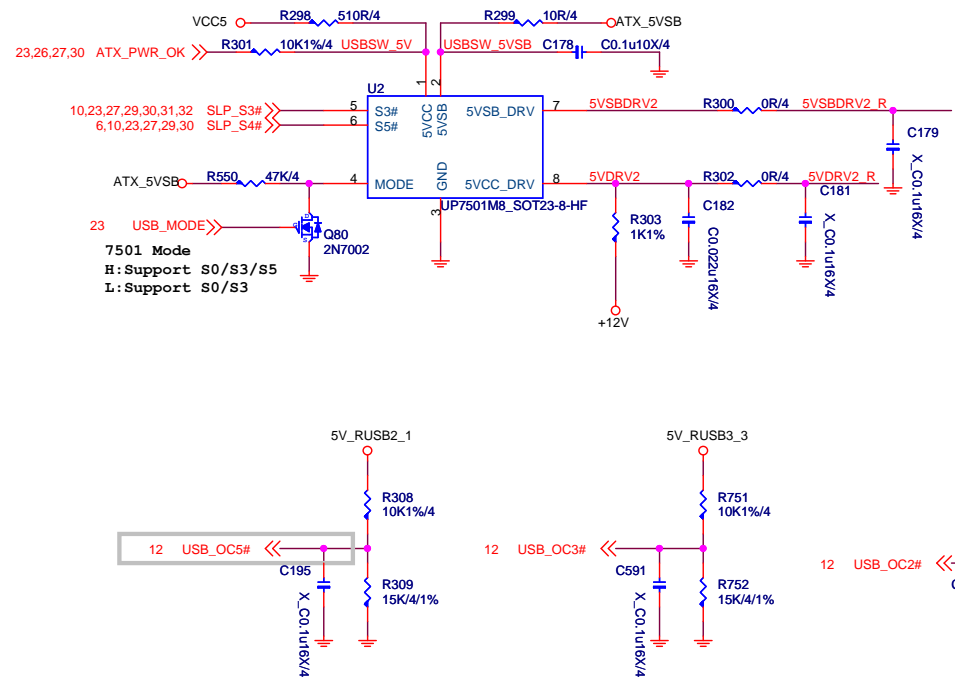


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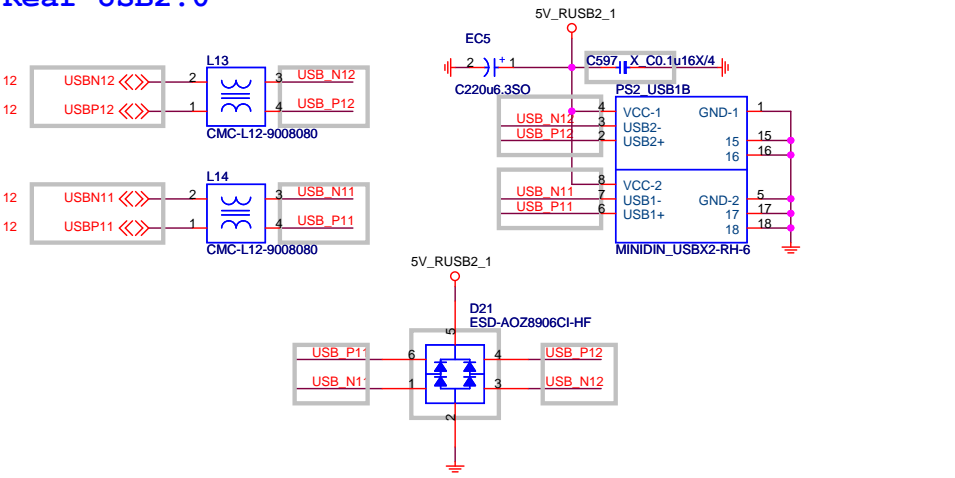
Size C	Document Description <b>Front/Rear USB3.0</b>	Rev 1.0
Date: Friday, September 30, 2016		Sheet 19 of 36

Rear/Front USB 3.1/3.0/2.0 Power

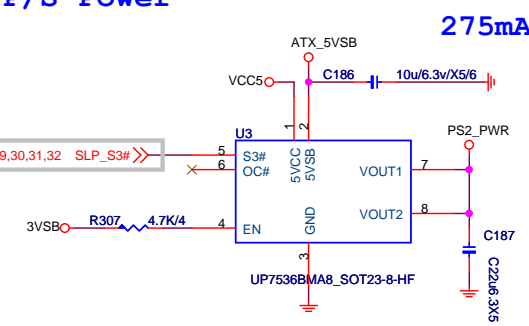



- 1A(rear USB2.0x2)
- 1.8A(rear USB3.0x2)
- 1.8A(rear USB3.0x2)
- 1.4A(front USB3.0x2)
- 1.8A(front USB3.1x1)
- 1.8A(rear USB3.0x2)

Rear USB2.0



P/S Power



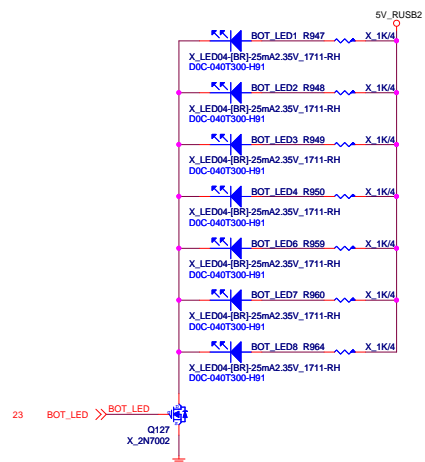


**MICRO-STAR INT'L CO.,LTD**

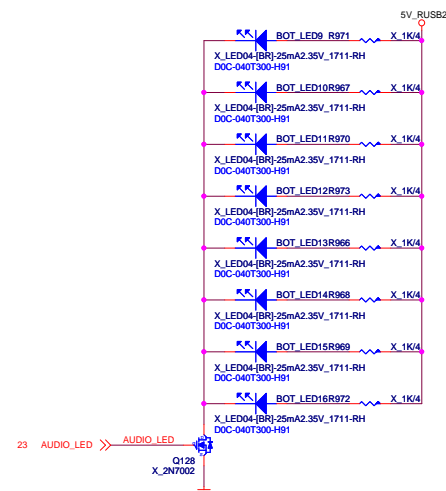
**MS-B9091**

Size B	Document Description	Rev 1.0
Rear USB2.0 / USB&P/S2 Power		
Date: Thursday, September 29, 2016	Sheet 20 of 36	

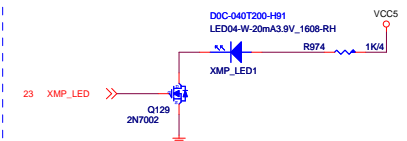
place near 4 corner of PCB.



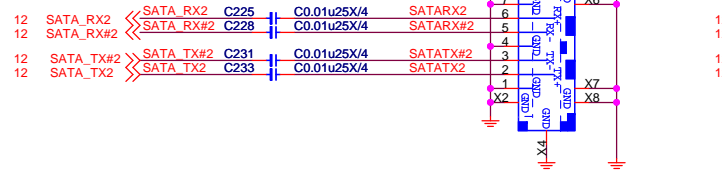
place near AUDIO line.



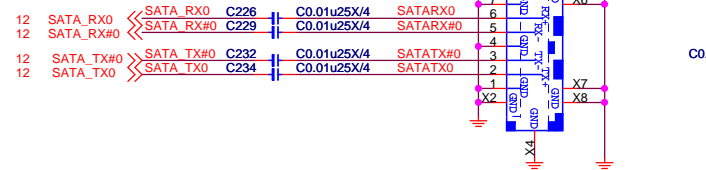
place near DIMM1.



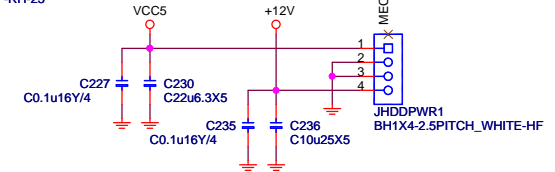
## SATA 3.0 Port 2



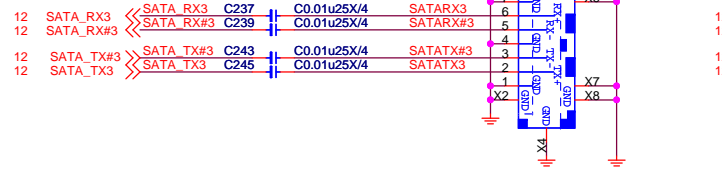
## SATA 3.0 Port 0



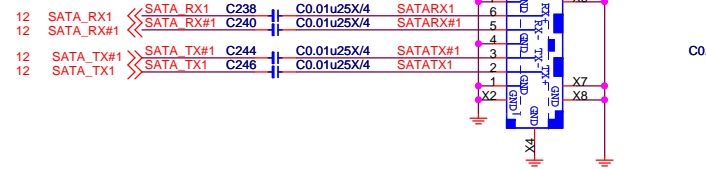
## SATA Power



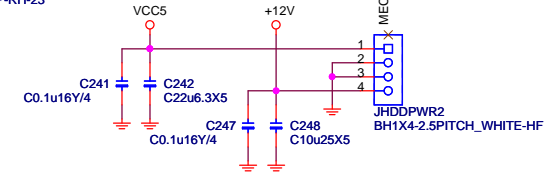
## SATA 3.0 Port 3



## SATA 3.0 Port 1



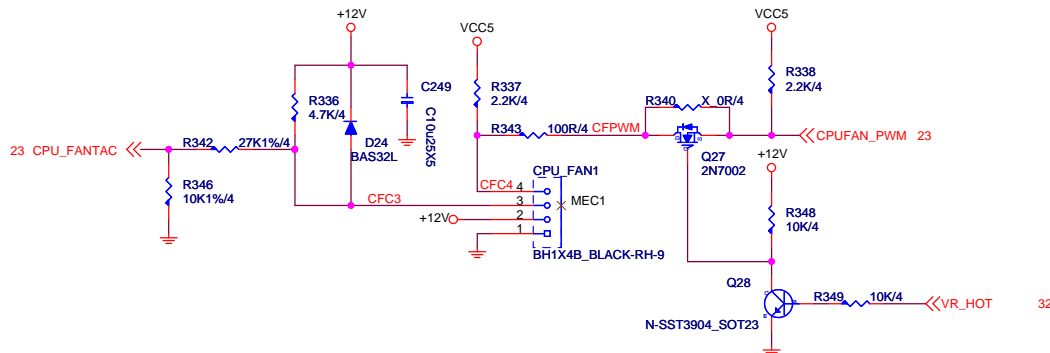
## SATA Power



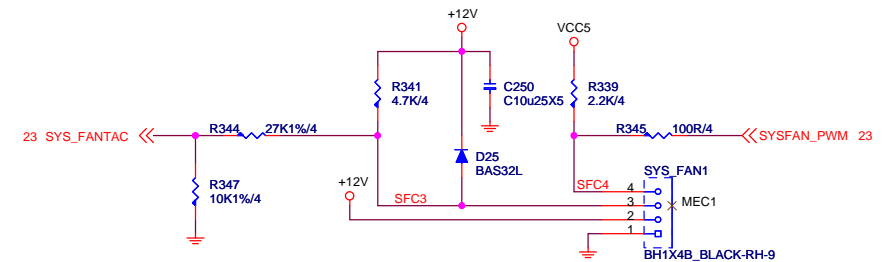
3.5 12V starup 2A,5V operat 0.51A 1pcs  
2.5 5V startup 1A 1 pcs

B902 max 3.5\*2+2.5\*2 current=12V/4A,5V/3A

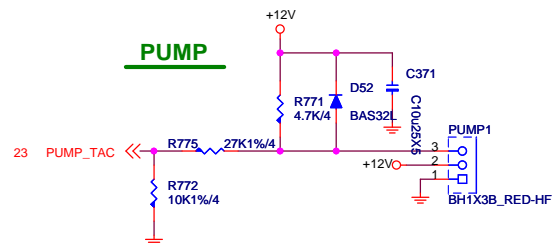
## CPU FAN



## SYS FAN



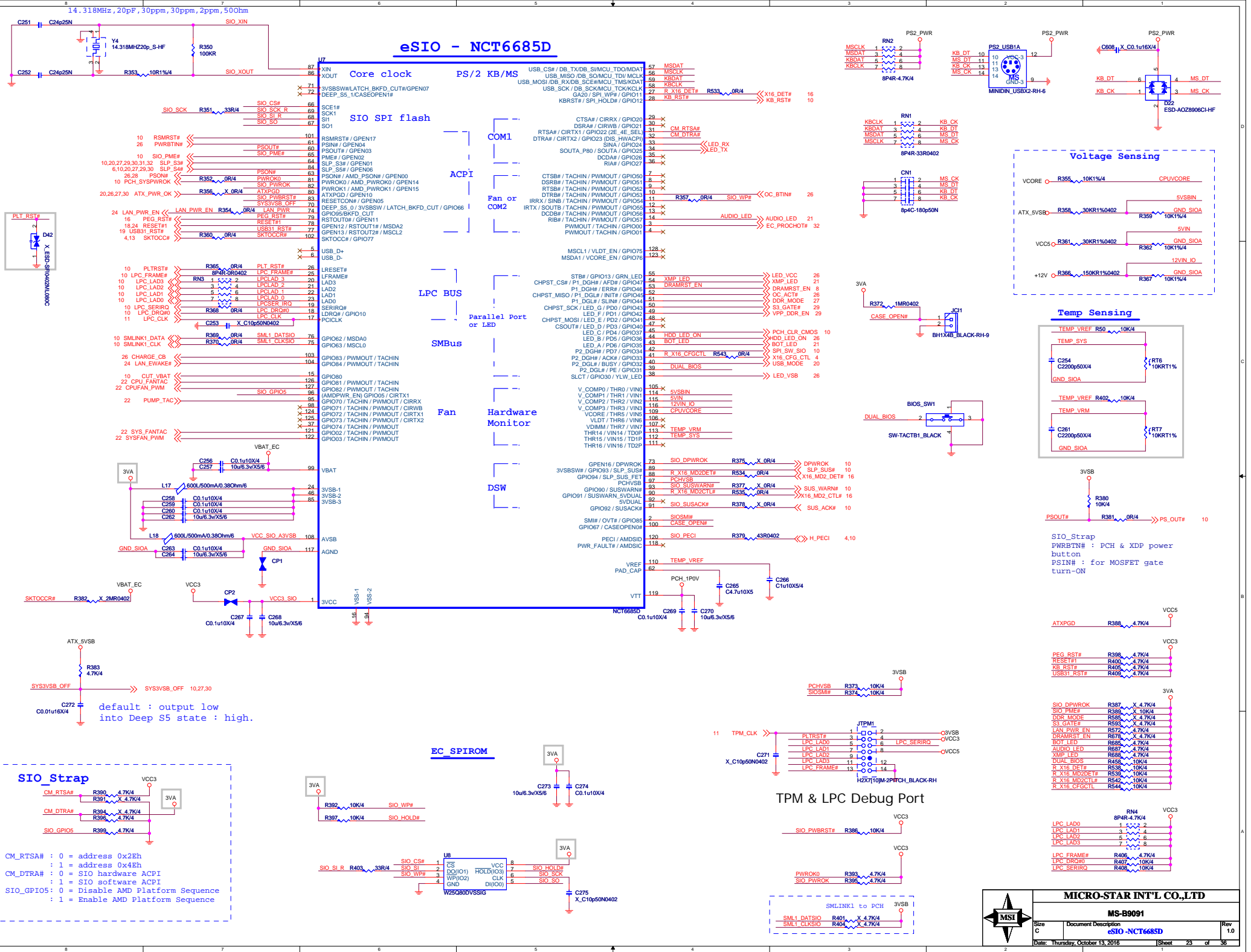
## PUMP



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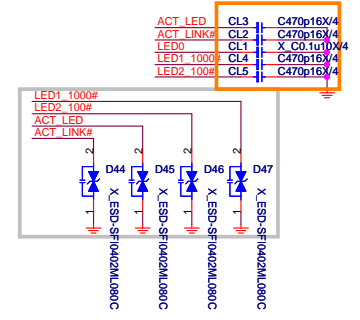
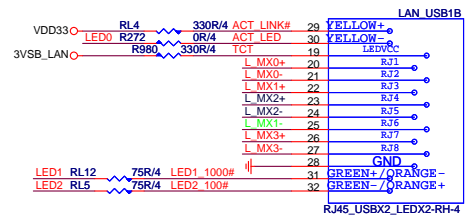
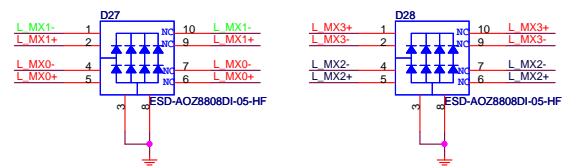
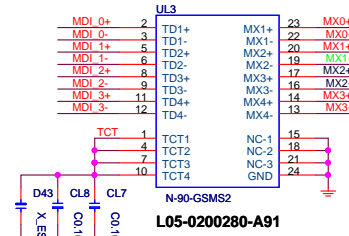
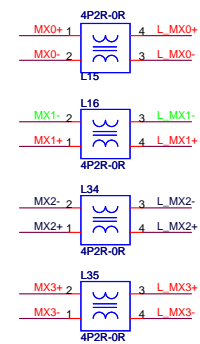
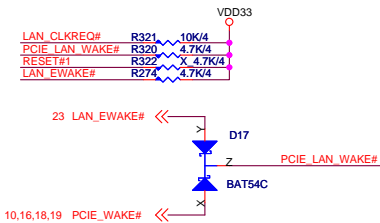
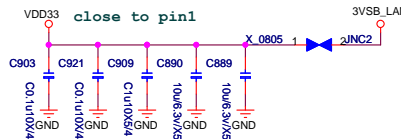
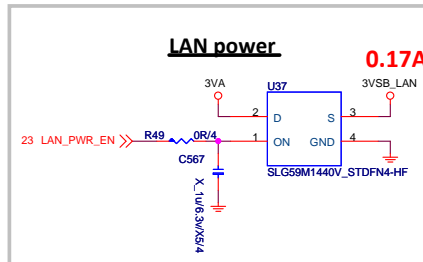
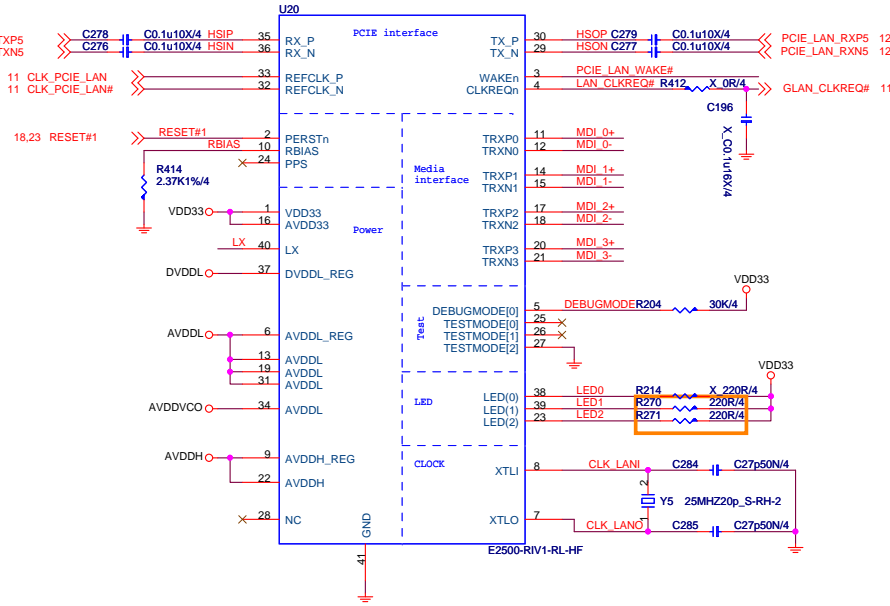
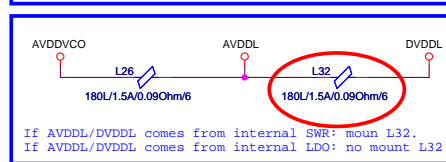
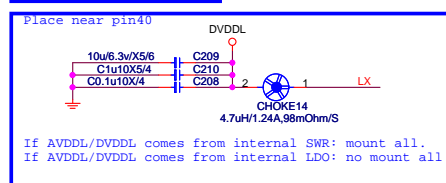
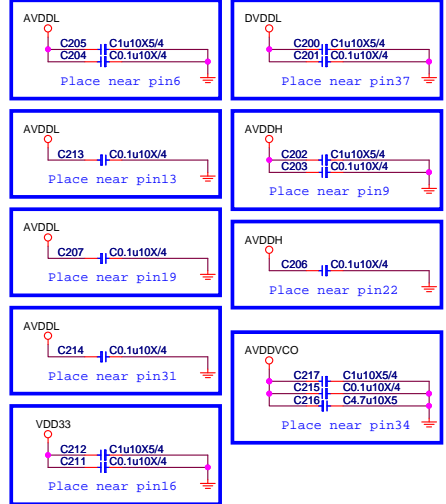
Size	Document Description	Rev
Custom	SATA Port & FAN	1.0
Date: Thursday, September 29, 2016	Sheet 22 of 36	

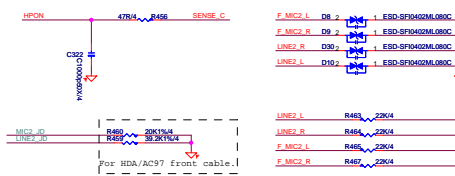
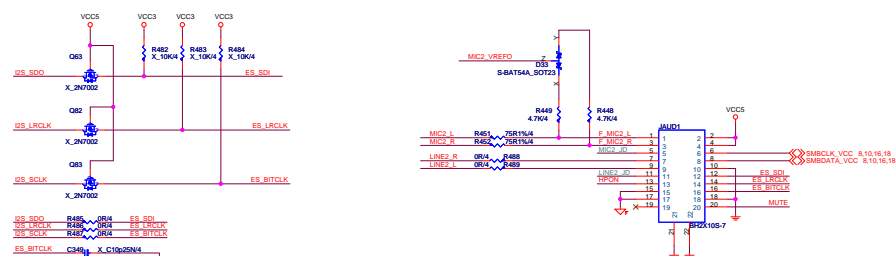
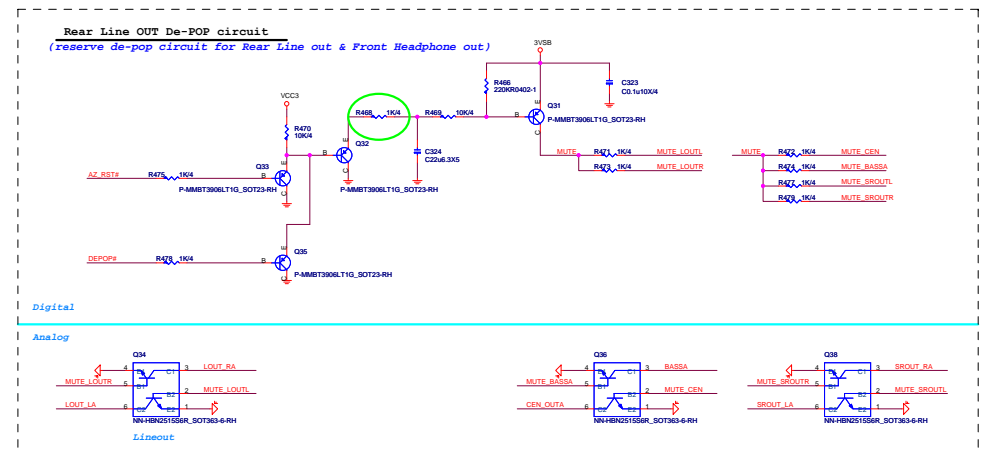
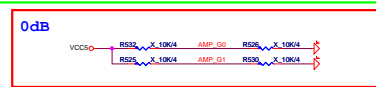
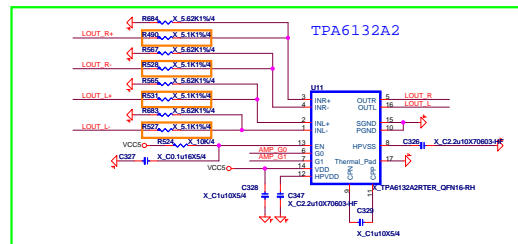
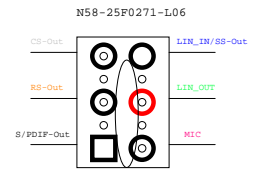
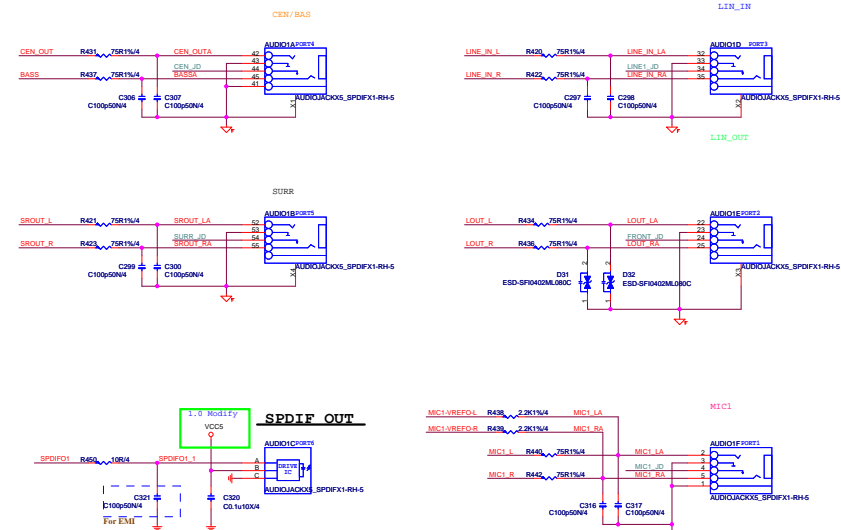


# E2400 Giga LAN

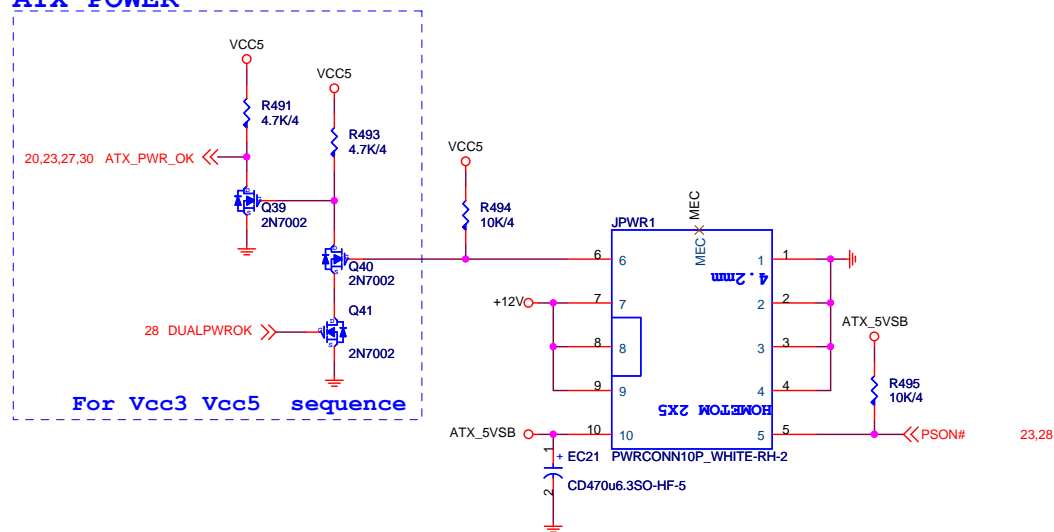
Gen1 2.5G  
Gen2 5G  
Gen3 8G  
Gen4 16G

VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDDIO power trace should be wider than 30mils;  
VDDIO\_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.

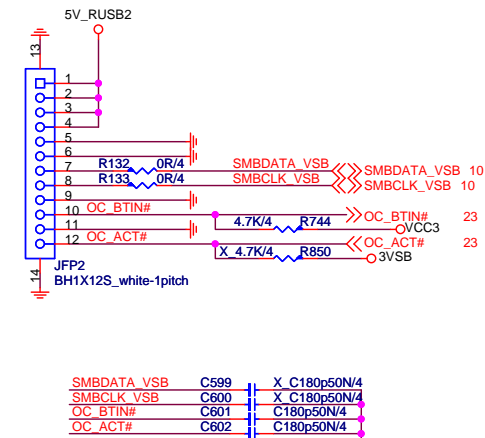




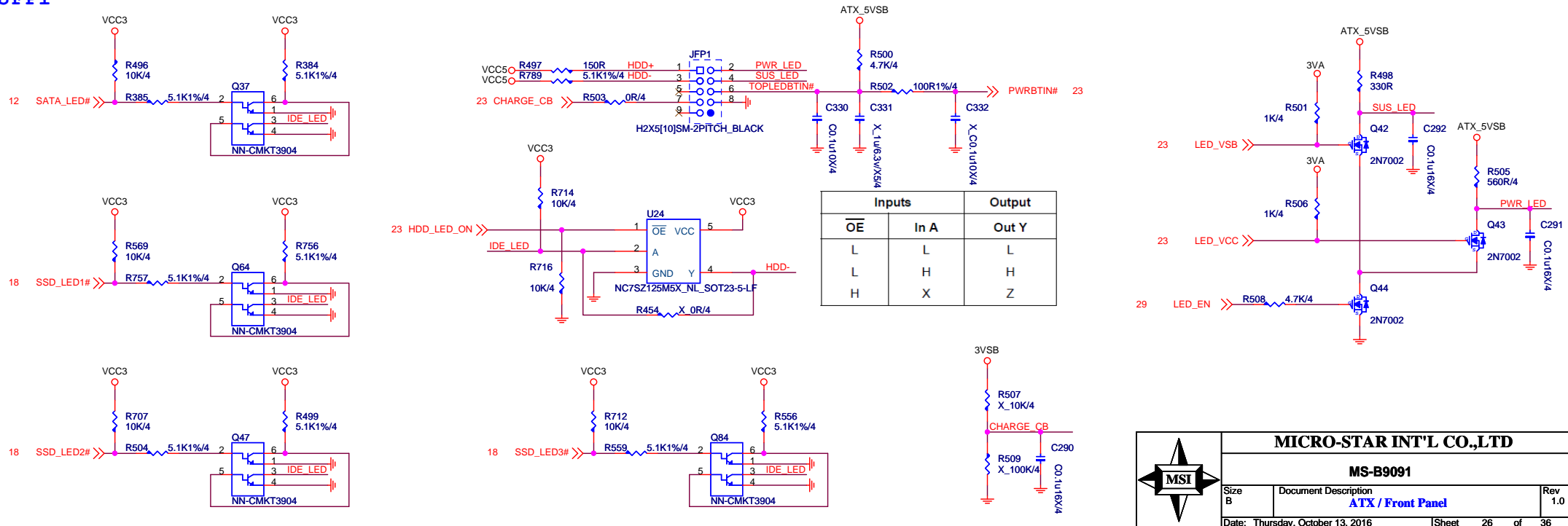
## ATX POWER



JFP2 → OC BTN&LED control



**JFP1**



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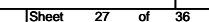
Size B	Document Description <b>ATX / Front Panel</b>	Rev 1.0
Date: Thursday, October 13, 2016		Sheet 26 of 36

1



ce

3VSB



total:15.6A

total:14.8A

OCP=30A  
OCP=27A

current leakage

23.26 PSON#

EMI

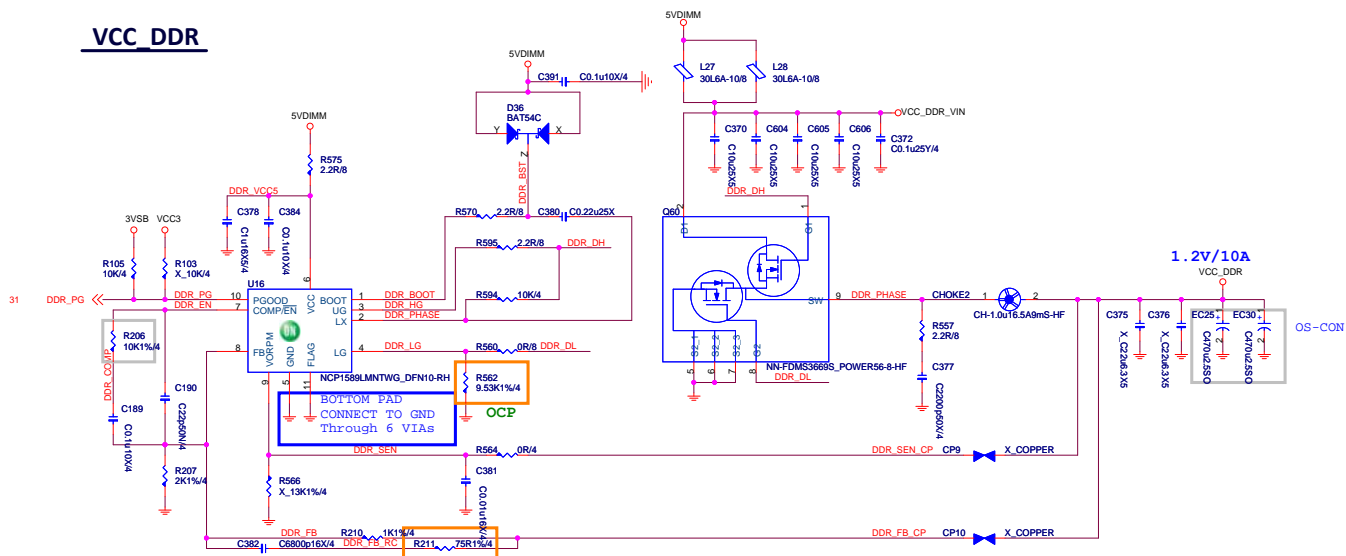


MICRO-STAR INT'L CO.,LTD

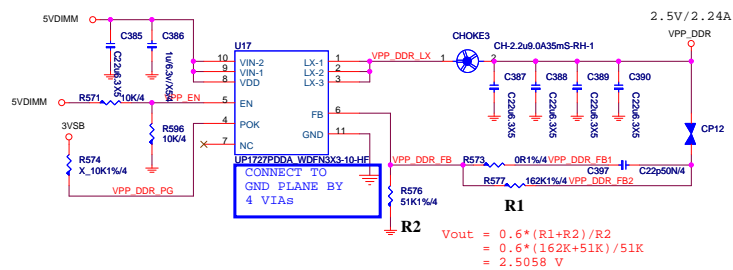
MS-B9091

Size Custom	Document Description 3V/5V (TPS51125RGER)	Rev 1.0
Date: Thursday, September 29, 2016 Sheet 28 of 36		

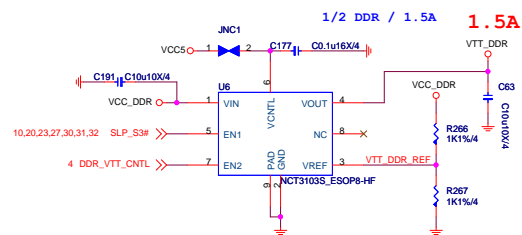
**VCC\_DDR**



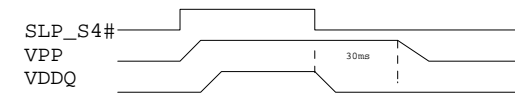
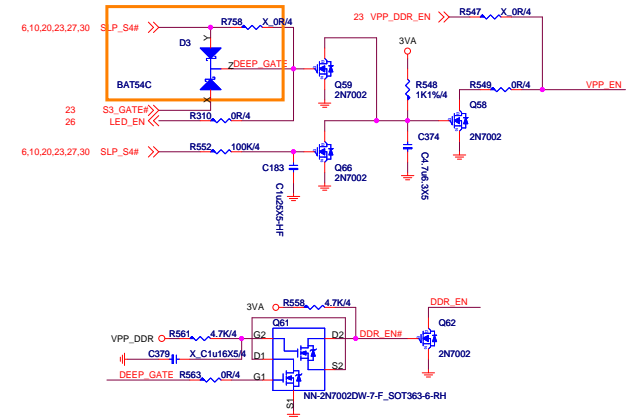
## VPP DDR



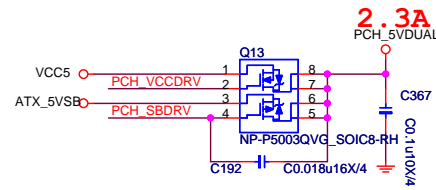
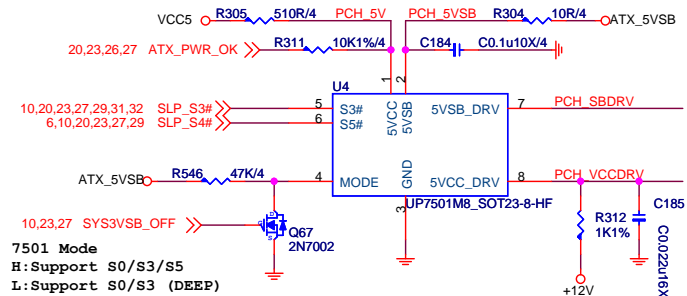
VTT\_DDR



### VPP\_DDR & VCC\_DDR Enable Control

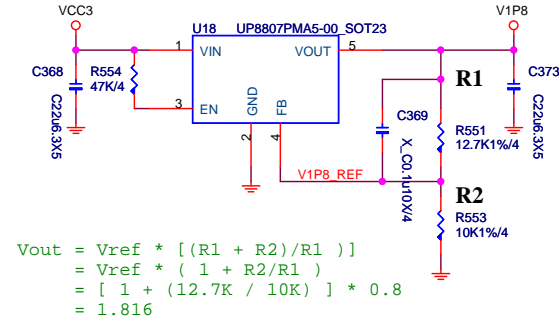


## PCH\_5VDUAL

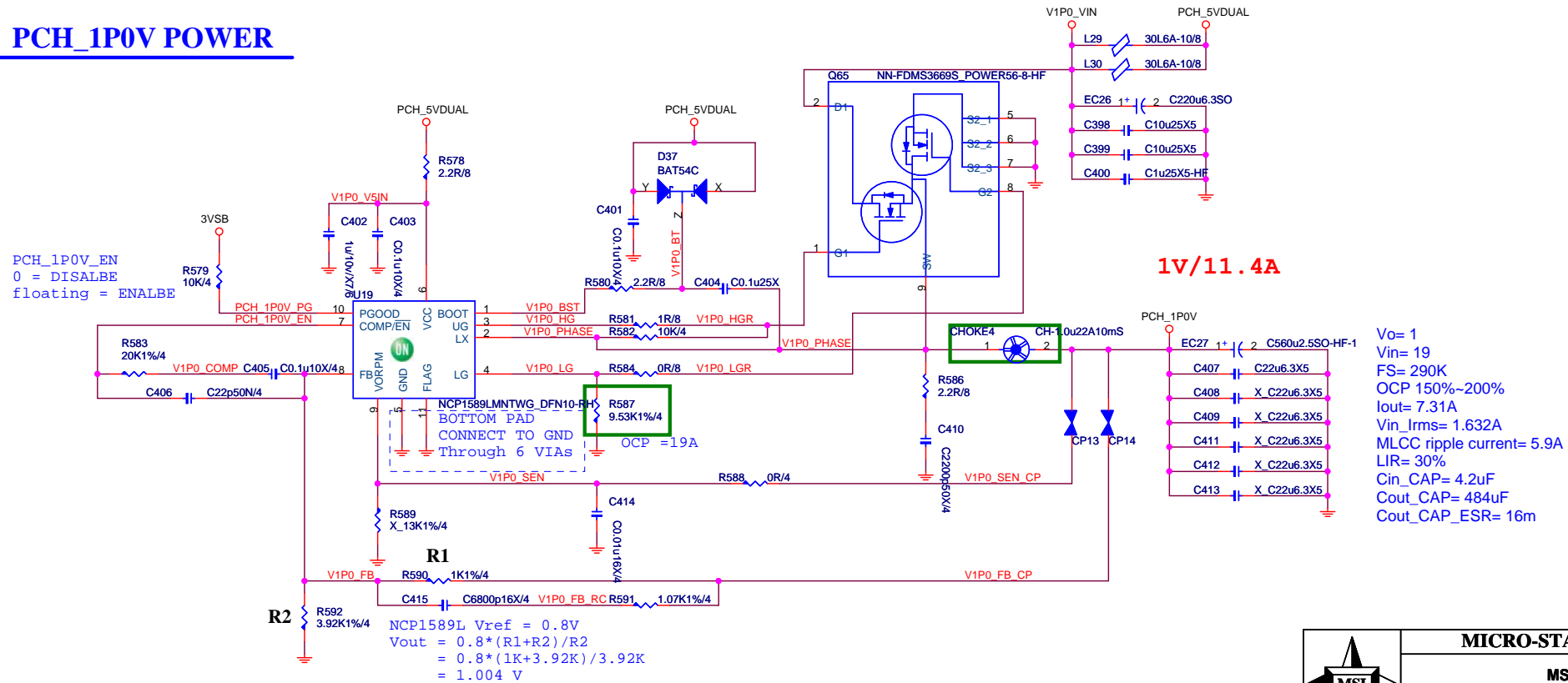


## V1P8

1.8V/0.5A



## PCH\_1P0V POWER

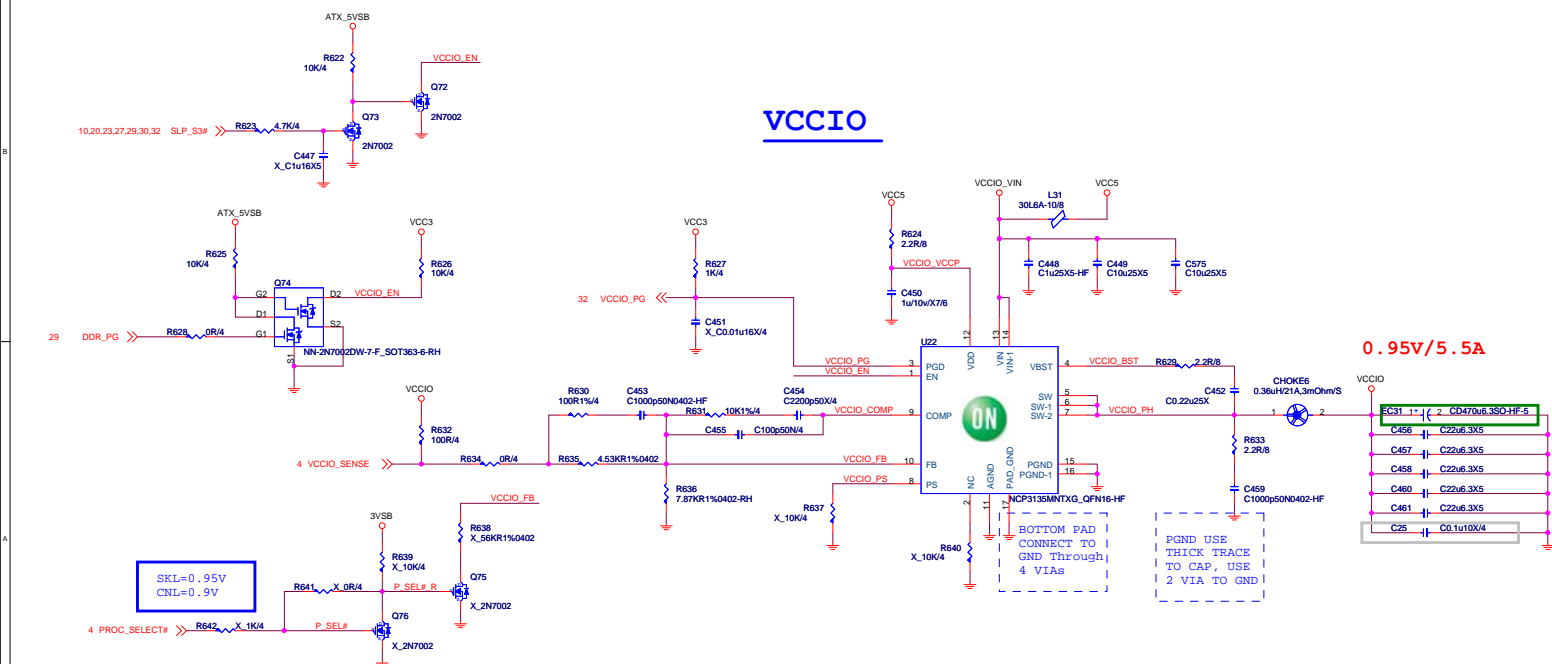
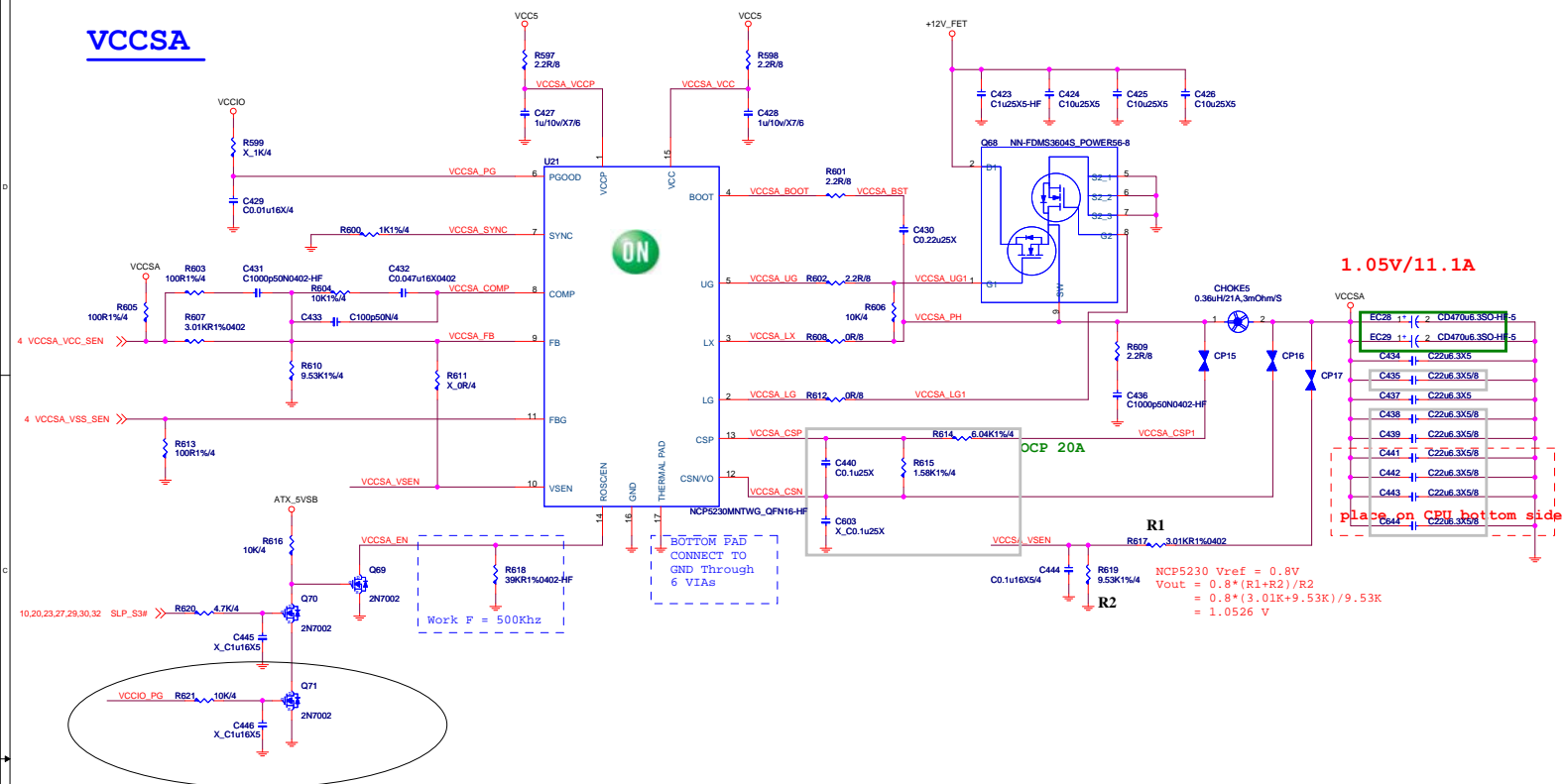


MICRO-STAR INT'L CO.,LTD

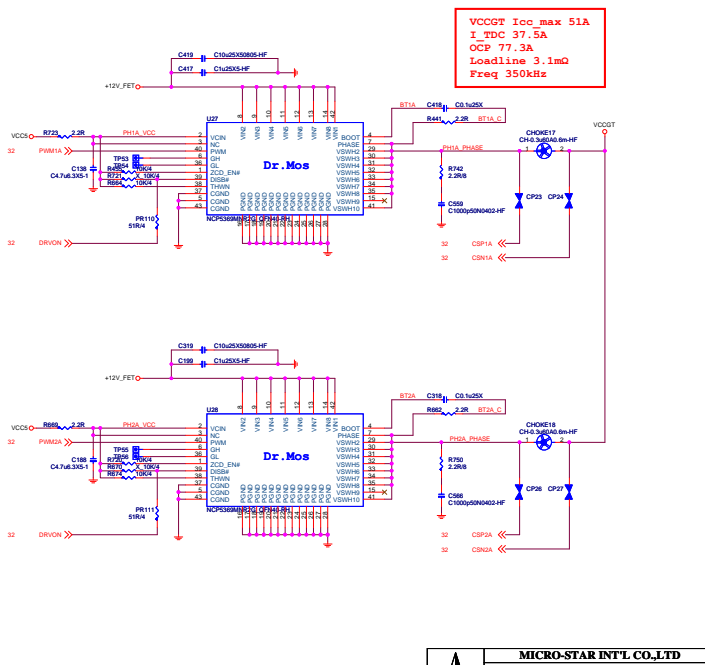
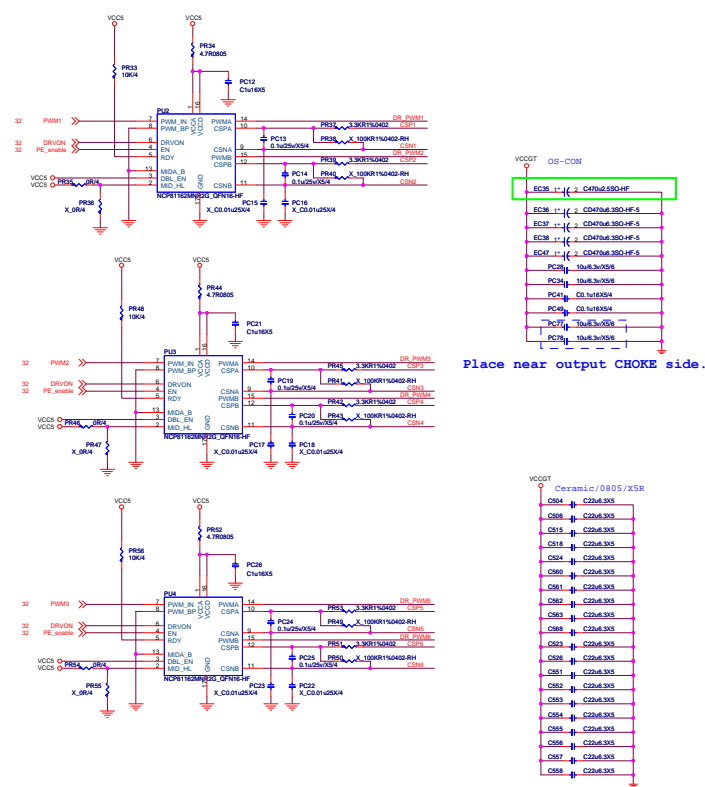
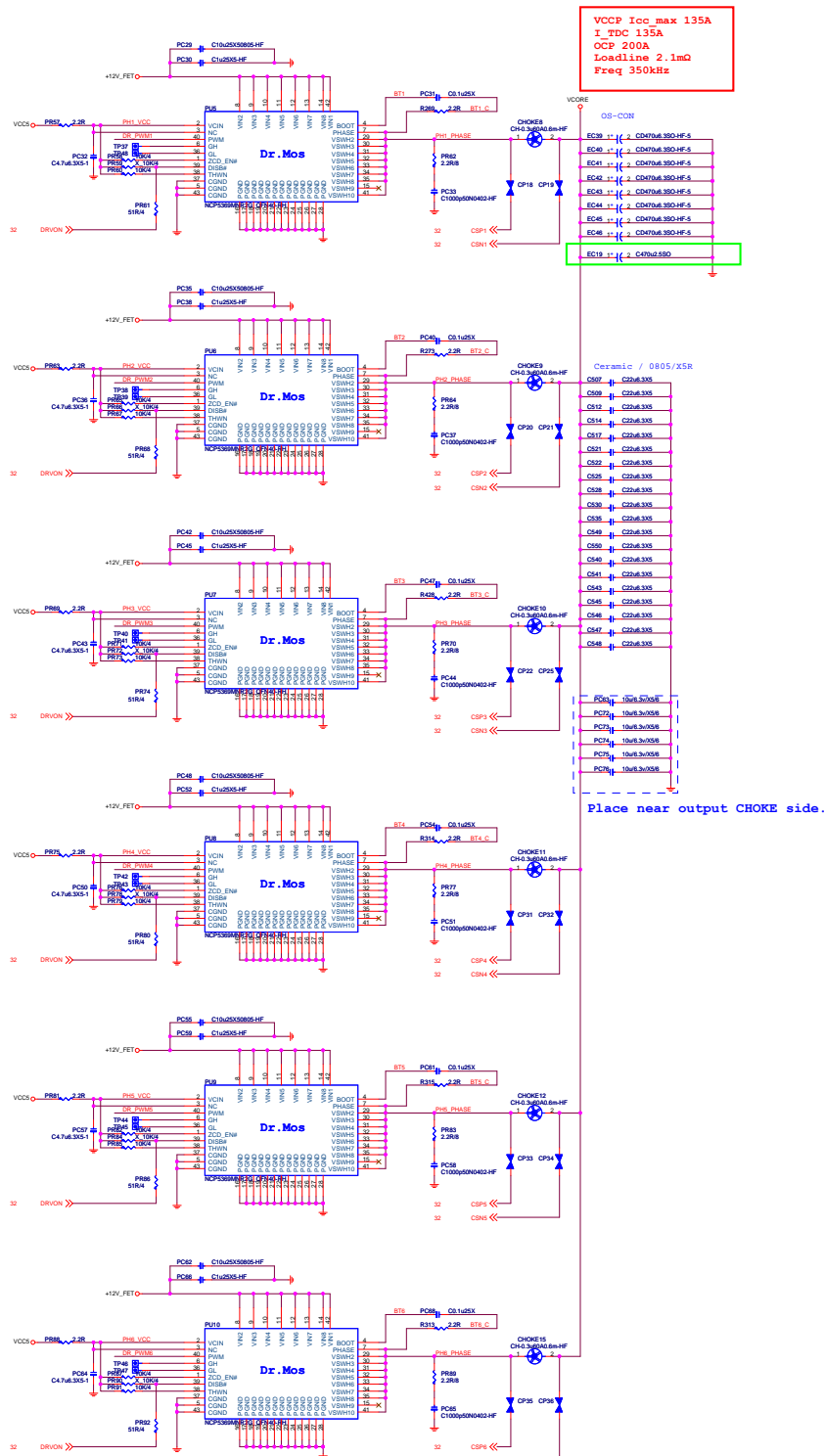
MS-B9091

Size	Document Description	Rev
B	PCH_1P0V / V1P8	1.0
Date:	Thursday, September 29, 2016	Sheet 30 of 36

**VCCSA**





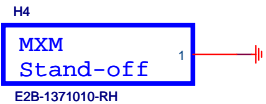
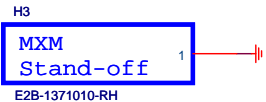


MICRO-STAR INT'L CO., LTD.

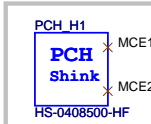
MS-89091

Doc. Name: Document No. VCCORE MOS / VCCGT MOS  
Date: Feb, September 20, 2016  
Rev: 38

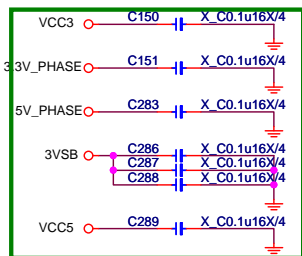
## SB\_SINK Stand-off



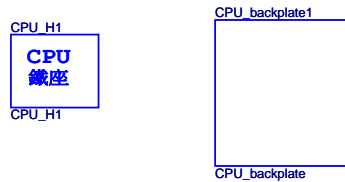
Stand off change to E2B-1371010-A89



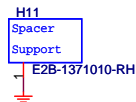
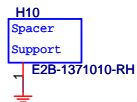
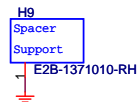
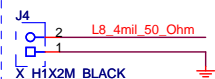
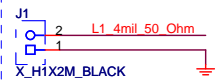
## BIOS label



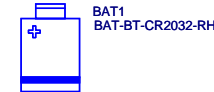
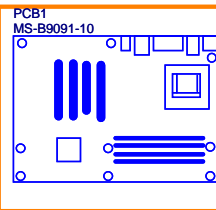
## CPU SOCKET



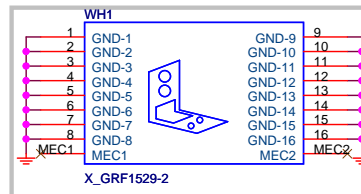
### Single End 50ohm



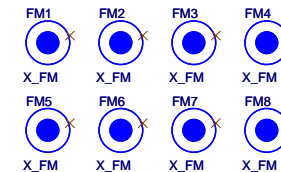
Add additional screw for PWM MOSFET heatsink.



9/14 change to D06-0105301-K26

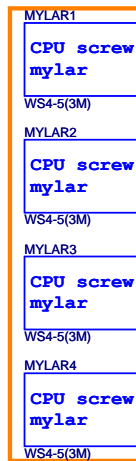
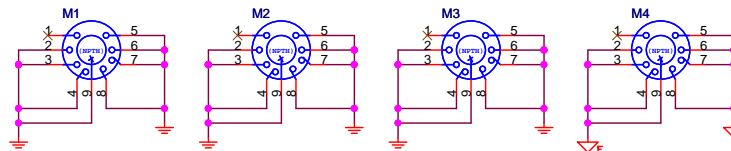


## Optical Fiducial Marks-120



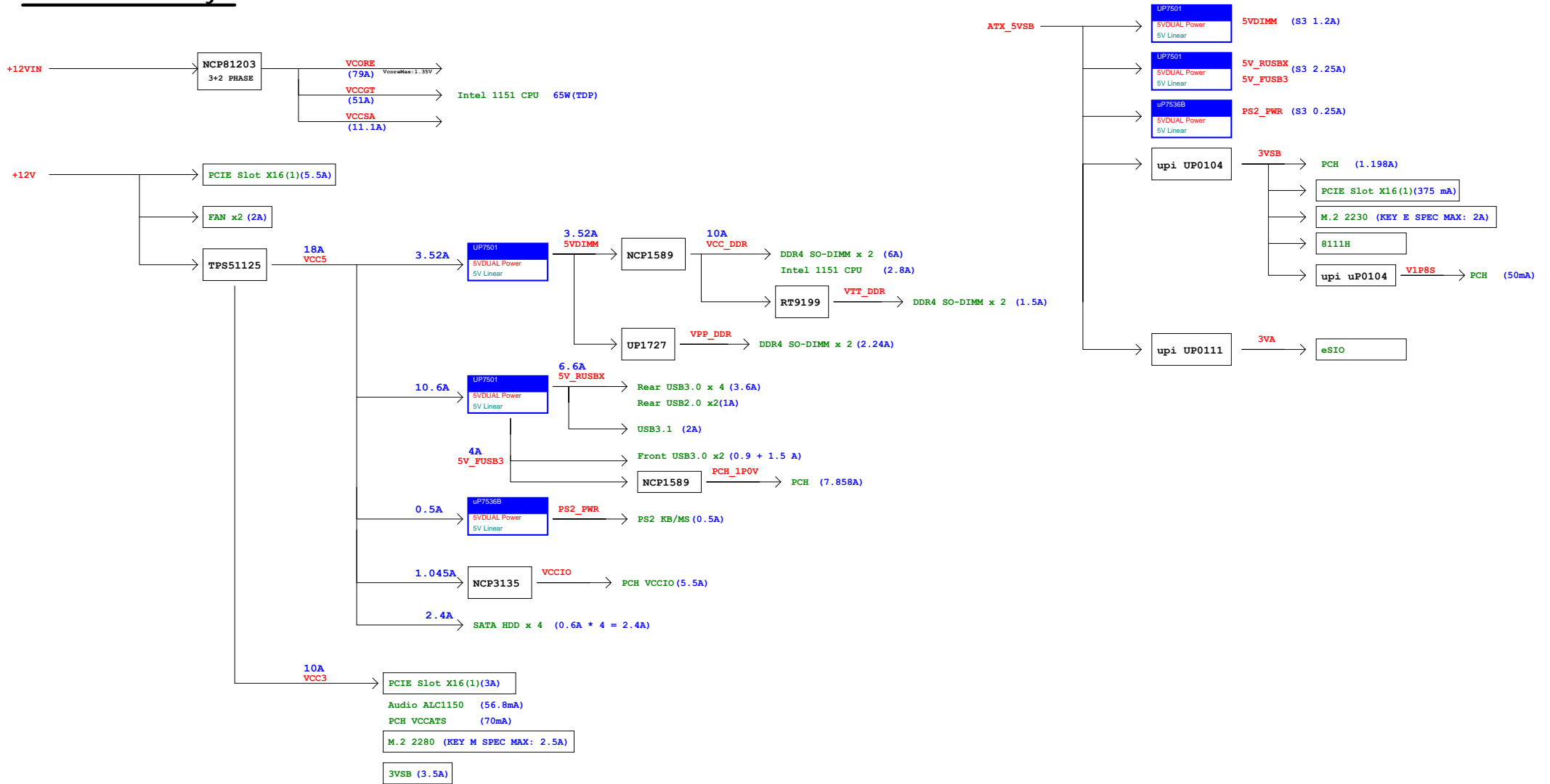
footprint change to H\_R276D157\_V8\_2

## Mounting Holes



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# Power Delivery



0A to 1.0

- 1. C(648,649,652,655) need change to 0.22uF due to B902A support ASM2142 GEN3.
- 2. modify anti-pop circuit.(use codec pin2/gpio0)
- 3. JPWR1 need rotate 180
- 4. Add clear MOS button (BIOS\_SW1) on WH1.
- 5. B9091 0A POWER SOLUTION
  - PC70 change to 330pf P/N: C11-3311812-W08
  - PR101 change to 32.4k 0402 1%
  - PC56 change to 120pF P/N: C11-1211012-W08
  - PC71 change to 820pF P/N: C11-8212012-W08
  - R635 change to 4.53K 0402 1%
  - R943 change to 15.4K 0402 1%
- 6. thermal team requirement
  - VRM MOS heatsink stand-off (H9/H10/H11) PN change to E2B-1371010-A89 due to Lack of height.
- 7. remove Fintek LED controller
- 8. R487 signal AZ\_BITCLK change to U10 pin12 I2S\_SCLK.
- 9. modify JFP2 to meet B909B pin define.(change to N32-1120040-H06 )
- 10. un-stuff Bottom side LED.
- 11. PCIEX16 change to non-latch part.
- 12. reserve 3 pin from PCIEX16 for new raiser card support.
  - 1. X16 present pin to EC for card detect
  - 2. add MD2 detect pin to EC.
  - 3. EC add a control pin to switch.
  - 4. H\_CFG5/H\_CFG6 connect to ec and control by EC.
  - added net:X16\_MD2\_CTL#/X16\_MD2\_DET#/X16\_CFG\_CTL/X16\_DET#
- 13. EC14 change to C71-101162E-S03 due to ME interference.
- 14. follow 200 series change caps type.
  - 1. EC32,EC33,EC34,EC51 change to C71-10116X1-N07
  - 2. EC1 change to C71-27117P1-N07
  - 3. EC39,EC40,EC41,EC42,EC43,EC44,EC45,EC46,EC35,EC36,EC37,EC38,EC47,EC28,EC29,EC31,EC21 change to C71-47106M1-N07